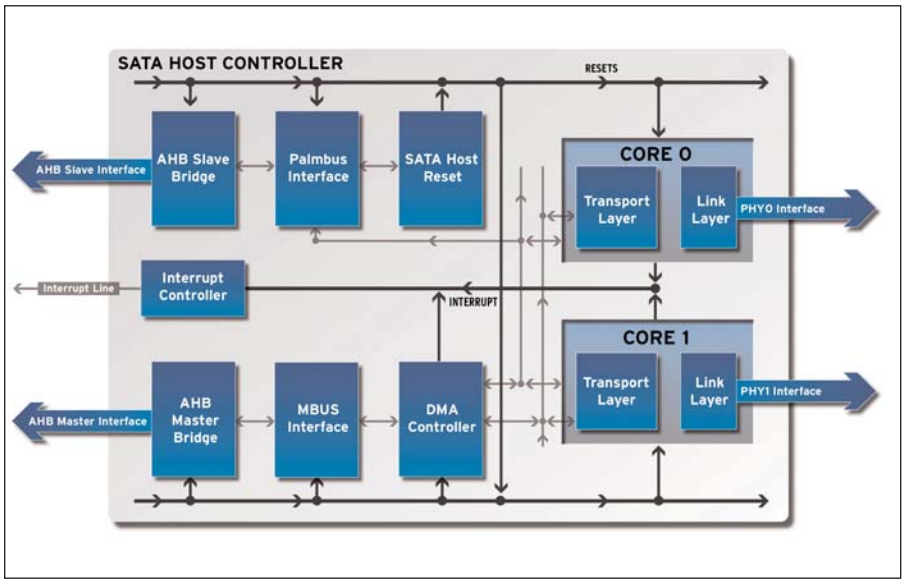
# Serial ATA IP - Host Controller




*The Mentor Graphics Serial ATA Host Controller is configured with two controllers for master/slave emulation. One controller can be easily removed for single point-to-point applications.*

## SATA Host Interface Controller

The Mentor Graphics® Serial ATA (SATA) Host Controller provides an efficient and easy-to-use interface to SATA devices. The core implements transfer speeds of either 150 MB/s or 300 MB/s and emulates programmable I/O, multi-word direct memory access (DMA), and Ultra ATA modes of operation. The core interface to the SoC includes a DMA controller to optimize data transfers to and from the IDE devices and provides PIO access via shadow registers. For ease of integration, the core includes a register set that it compatible with the Intel chip set.

Mentor's SATA Host Controller is designed to connect to the host processor by either the CoreFrame bus interface or the AMBA AHB 2.0 slave interface. It supports memory through the CoreFrame or the AMBA AHB 2.0 master interface.

### Major product features:

- Compliant with the Serial ATA specification version 2.6
- Supports 1.5 Gb/s (150 MB/s) or 3 Gb/s (300 MB/s) speeds
- Supports Native Command Queuing (NCQ)
- Support for Spread Spectrum Clocking (SSC)
- Descriptor-based, scatter-gather DMA engine
- Intel register set compatible
- Synchronous DMA interface for data transfers
- Supports 10-, 20-, or 40-bit SATA standard PHY interface
- Asynchronous Notification
- Supports either CoreFrame or AMBA AHB 2.0 bus interface

### Deliverables:

- Verilog RTL source code
- Example synthesis scripts
- Verilog functional verification environment with tasked-based verification and PHY model
- Detailed specifications including user guide, product specification, verification guide, and programmers guide

### Related products:

- **MSATA PHY S130A** - SATA PHY (up to 3Gbps) for SMIC 130nmG
- **MSATA PHY T130A** - SATA PHY (up to 3Gbps) for TSMC 130nm LVOD

## Signal Interface Signals

| System Interface Signals | | |
|---|---|---|
| Signal | Type | Description |
| CLK | Input | System Clock |
| TX_CLOCK | Input | SATA Clock |
| TESTMODE | Input | Scan Test mode |
| RST_N | Input | Power on Reset |
| PRIMARY_MODE | Input | Decode Access to primary (1) or secondary (0) addresses |
| IF_WIDTH | Input | Selects PHY interface width of 10, 20, or 40 bits |
| MAS_SLV | Input | Master/Slave Selection |
| OVER_CLOCK | Input | Over Clocking Enable |
| INTR | Output | Interrupt Signal |
| AHBM_ERROR | Output | AHB Interface Error Flag (debug) |
| AHB Master Interface Signals | | |
| HRDATA_M[31:0] | Input | AHB Master Read Data Bus |
| HREADY | Input | AHB Master Ready |
| HGRANT_M | Input | AHB Master Bus Grant |
| HRESP_M[1:0] | Input | AHB Master Transfer Response |
| HBUSREQ_M | Output | AHB Master Bus Request |
| HADDR_M[31:0] | Output | AHB Master Address Bus |
| HWDATA_M[31:0] | Output | AHB Master Write Data Bus |
| HWRITE_M | Output | AHB Master Write Signal |
| HSIZE_M[2:0] | Output | AHB Master Burst Size |
| HBURST_M[2:0] | Output | AHB Master Burst Type |
| HTRANS_M[1:0] | Output | AHB Master Transfer Type |
| HLOCK_M | Output | AHB Master Bus Request Lock |
| AHB Slave Interface Signals | | |
| HADDR_S[31:0] | Input | AHB Slave Address Bus |
| HWDATA_S[31:0] | Input | AHB Slave Write Data Bus |
| HTRANS_S[1:0] | Input | AHB Slave Transfer Type |
| HSEL_S | Input | AHB Slave Select Line |
| HWRITE_S | Input | AHB Slave Write Signal |
| HSIZE_S[2:0] | Input | AHB Slave Burst Size |
| HRDATA_S[31:0] | Output | AHB Slave Read Data Bus |
| HREADY_OUT | Output | AHB Slave Output Ready Line |
| HRESP_S[1:0] | Output | AHB Slave Transfer Response |
| PHY Interface Signals | | |
| RX_CLOCK_0/1 | Input | Receive Data Clock Master/Secondary |
| PL_DATA_0/1 [x:0] | Input | Receive Data Master/Secondary |
| PHYRDY_0/1 | Input | PHYRDY Signal Detected Master/Secondary |
| COMWAKE_0/1 | Input | COMWAKE Detected Master/Secondary |
| COMINIT_0/1 | Input | COMINIT Detected Master/Secondary |
| SPDMODE_0/1 | Input | Speed Setting Master/Secondary |
| PHY_INT_ERR_0/1 | Input | Internal PHY error detect Master/Secondary |
| LL_LP_DATA_0/1 [x:0] | Output | Transmit Data Master/Secondary |
| PHY_RST_N_0/1 | Output | PHY Reset Signal Master/Secondary |
| SCR_SPDSEL_0/1 | Output | Speed Setting Output Master/Secondary |
| SCR_NEARAFELB_0/1 | Output | Parallel Loopback Enable Master/Secondary |
| TL_FARAFELB_0/1 | Output | Serial Loopback Enable Master/Secondary |
| LL_PARTIAL_0/1 | Output | Partial Power Mode Enable Master/Secondary |
| LL_SLUMBER_0/1 | Output | Slumber Power Mode Enable Master/Secondary |

*M/S = Master/Secondary

## Functional Description

The Serial ATA Host Controller core is designed to interface to a host CPU and DMA interfaces on one end, and the Serial ATA Physical Layer on the other end.

The Transport Layer Controller and the Link Layer Controller are the two core submodules that control the overall operation. The Link Layer Controller controls the operations relating to the host platform. Both controllers coordinate their actions and utilize resources to transfer data between a host system and a SATA Physical Layer core like one of Mentor Graphics MSATA PHY products for either TSMC or SMIC processes.

The Link Controller interacts directly with the SATA PHY to coordinate serial transfers. It generates and checks CRC, scrambles/descrambles data, performs encoding/decoding, and manages primitive transmission and receipt.

The Transport Layer is used to store the headers of incoming and outgoing packets. Data, Status, and Vendor-specific Packet Headers sent to and from the device are stored in the FIS buffers, which are part of the Transport Layer.

## Reference Technology Gate Count:

- 34,500 gates

**Visit our website at www.mentor.com/ip for additional product information.**



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