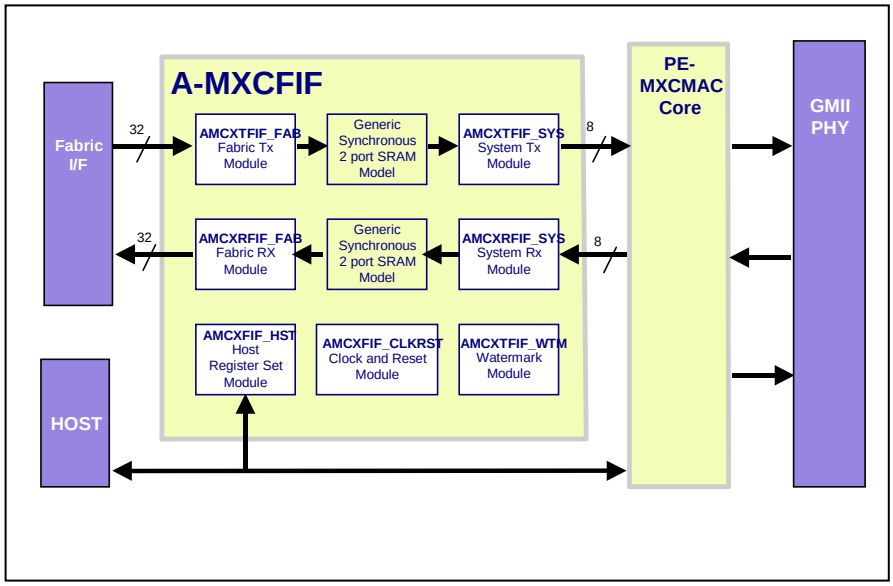
A-MCXFIF™

FIFO Memory Interface for the PE-MCXMAC™

Inventra™ Soft Core (RTL IP)

D A T A S H E E T



A-MCXFIF Application

Overview

The A-MCXFIF™ is a flexible FIFO module with transmit and receive buffering, which can significantly improve the performance of embedded 10/100/1000 Mbps Ethernet systems. It integrates with the PE-MCXMAC™ 10/100/1000 Mbps Ethernet MAC module (also available from the Mentor Graphics Inventra Soft Core Library) and functions in all of the PE-MCXMAC's modes.

The A-MCXFIF is a low gate count, easily synthesizable FIFO module that offers increased system level throughput through allowing data queuing. Automatic pause frame handshaking and per transmit frame MAC configuration data are both supported.

Other features of this logic module are clock-frequency-independent I/O ports, single or multiple word I/O data transfers, and full memory utilization with graceful memory full frame drop. The A-MCXFIF module also provides programmable high and low receive storage level indicators and pause frame handshaking re-assertion intervals, high transmit storage level indication, and CPU frame insertion and inspection capabilities.

The A-MCXFIF module is provided in Verilog RTL source code, with a full test suite and module level documentation. The A-MCXFIF uses synchronous dual-port memories.

Major Product Features:

- Operates at 10, 100 or 1000 Mbps
- Provides data queuing for increased system level throughput
- User definable storage sizes
- Clk frequency independent I/O ports
- Single or multiple word data transfers
- Programmable Rx and Tx storage level indicators, plus Tx storage under-run indication
- CPU frame insertion and inspection
- Automatic pause frame handshaking
- Programmable pause frame handshaking reassertion interval
- Graceful Rx memory full frame drop
- Graceful enable and disable
- Programmable frame or word cut-through threshold
- Tx storage frame rewind capabilities
- Full memory utilization
- Optional per transmit frame MAC configuration data supported
- Low gate count
- Fully synthesizable
- Scan insertion-friendly design
- Uses synchronous dual-port memories

Deliverables:

- Verilog RTL source code
- Functional testbench
- Synopsys constraint files
- Module-level documentation

Mentor Graphics is the leading supplier of a broad range of IP soft cores targeting standards-based communications applications. These highly re-usable cores help systems and chip designers get to market faster.

Structure

The A-MCXFIF consists of the following seven major RTL logic sub-modules:

AMCXTFIF_FAB
FIFO Fabric Transmit Interface Module

AMCXTFIF_SYS
FIFO System Transmit Interface Module

AMCXRFIF_FAB
FIFO Fabric Receive Interface Module

AMCXRFIF_SYS
FIFO System Receive Interface Module

AMCXTFIF_WTM
FIFO System Watermark module

AMCXFIF_HST
FIFO Host Interface Module

AMCXFIF_CLKRST
FIFO Clock and Reset Module

Implementation

The A-MCXFIF module and the PE_MCXMAC core have been optimized for use in multiple-MAC applications. These include switches, multi-port-port interface cards, NICs and routers. The exact nature of the common sections for system data transport, address recognition and statistics will be application dependent, but the PE-MCXMAC and A-MCXFIF cores have enough built-in flexibility to cover almost any system concept.

Host Interface Options

The A-MCXFIF module and the PE_MCXMAC core connect to a host system.

The host system may be of different types. In a switch system, the host will generally be the embedded CPU or the back plane switching fabric.

Testbenches

The A-MCXFIF is supplied with two testbenches, one which verifies the A-MCXFIF when not integrated with the PE-MCXMAC, and one which verifies their operation together. Each testbench is described in a separate Verification document.

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Signal Description

Clock and Reset Signals	
External hard reset; Reset bypass	Input
A-MCXMAC transmit clock (post tree)	Input
A-MCXFIF Fabric Tx clock (post tree)	Input
A-MCXMAC receive clock (post tree)	Input
A-MCXFIF Fabric Rx clock (post tree)	Output
Host I/F Signals	
Host reset	Input
Host clock	Input
Host chip select not	Input
Host read / write not	Input
Host address	Input
Host input data	Input
Host output data	Input
Host output data enable	Output
System Transmit I/F Signals	
Transmit packet start of frame	Output
Transmit packet data	Output
Transmit packet end of frame	Output
Transmit packet under run	Output
Transmit packet control frame	Output
Transmit per packet override	Output
Transmit per packet pad mode; CRC mode	Output
Transmit packet need data	Input
Pause request	Output
Pause value	Output
Pause acknowledge	Input
Transmit packet retransmit	Input
Transmit packet abort	Input
Transmit Packet Slot Timer	Input
Transmit Half Duplex Flow Control	Output
System Receive I/F Signals	
AMCXMAC receive Clock enable	Input
Receive packet start of frame	Input
System Receive data	Input
Receive packet data valid	Input
Receive packet end of frame	Input
Receive packet drop frame	Input
Receive statistics vector + pulse	Input
Receive unicast address match	Input
Fabric Transmit I/F Signals	
Fabric transmit ready	Input
Fabric transmit accept	Output
Fabric transmit start of frame; end of frame	Input
Fabric transmit frame data	Input
Fabric transmit data not valid	Input
Fabric transmit per packet enable	Input
Fabric transmit per packet generate FCS	Input
Fabric transmit per packet pad mode	Input
Fabric transmit control frame	Input
Fabric transmit high watermark	Input
Fabric Receive I/F Signals	
Fabric receive accept	Input
Fabric receive start of frame; end of frame	Output
Fabric receive frame data	Output
Fabric receive data not valid	Output

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, OR 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

European Headquarters
Mentor Graphics Corporation
Immeuble le Pasteur
13/15, rue Jeanne Braconnier
92360 Meudon La Foret
France
Phone: 33-1-40-94-74-74
Fax: 33-1-46-01-91-73

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F,
International Trade Building
No.333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-2756027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

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