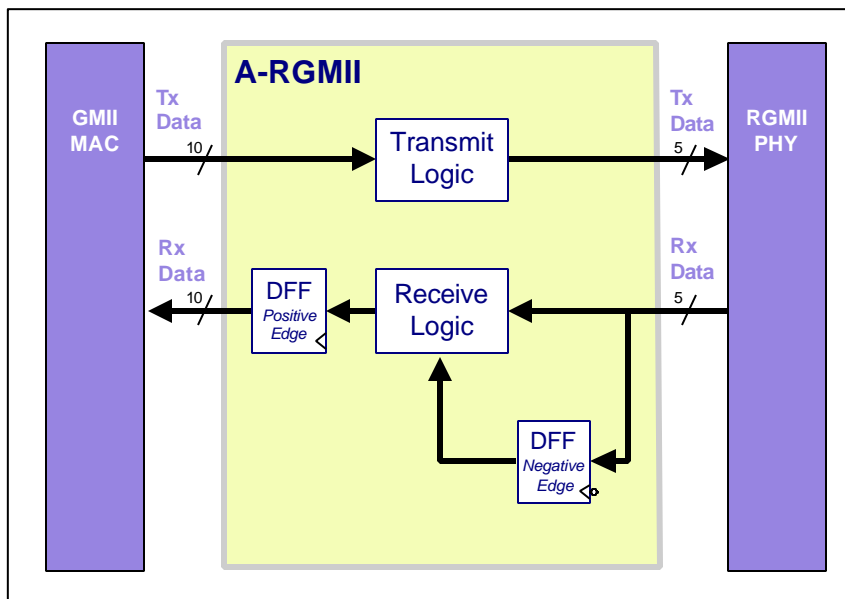


A-RGMII

Reduced Gigabit Media Independent Interface

Inventra™ Soft Core (RTL IP)

D A T A S H E E T



A-RGMII Sub-modules and Data Flow

Overview

The A-RGMII pack provides a reduced Gigabit Media Independent Interface that facilitates connection between any IEEE 802.3-standard GMII, MII or TBI interface and a RGMII interface that is compliant with V2.0 of the RGMII specification.

The main feature of the RGMII interface is that it offers a reduced pin-count interface to gigabit Ethernet PHYs. The A-RGMII thus allows devices such as the PE-GMAC0 Gigabit MAC and the PE-MCXMAC 10/100/1000 Mbps MAC to connect to reduced pin-count PHYs. (The PE-GMAC0 and PE-MCXMAC are both available from the Mentor Graphics Inventra™ range of soft cores.)

The required 10-signal interface to the PHY is provided by the ARGMI module within the A-RGMII pack. This module also performs the conversion of the 8-bit GMII data handled by the supported Gigabit MACs to/from the 4-bit data format of the RGMII interface in both the transmit and the receive directions.

There are many different possible applications, including Network Interface designs, Ethernet Switching designs and test equipment designs.

Major Product Features:

- Provides reduced pin-count interface to Ethernet physical layer devices
- Instance-based configuration for reduced post synthesis logic
- Supports Draft Version 2.0 of the RGMII Specification
- Supports TBI transfers
- Supports MII transfers
- Supports propagation of optional in-band status
- Supports 1 Gbps Half duplex operation
- Fully synthesizable
- Scan insertion-friendly design

Deliverables:

- Verilog source of ARGMI module
- Wrappers integrating ARGMI module with PE-GMAC0 and PE-MCXMAC
- Synthesis constraints files
- Functional testbench with documentation of conformance to appropriate IEEE PICS
- Design documentation

Related Products:

- PE-GMAC0 1 Gbps Ethernet MAC
- PE-MCXMAC 10/100/1000 Mbps Ethernet MAC

Mentor Graphics is the leading supplier of a broad range of IP soft cores targeting standards-based communications applications. These highly re-usable cores help systems and chip designers get to market faster.

A-RGMII: Reduced Gigabit Media Independent Interface Soft Core

Functional Overview

The A-RGMII pack provides a Reduced Media Independent Interface for Gigabit Ethernet MACs such as the PE-GMAC0 and PE-MCXMAC which offer a IEEE802.3 standard GMII, MII or TBI interface.

The interface between the 24-signal GMII interface and the 12-signal RGMII interface is provided by the ARGMMII module supplied within the A-RGMII pack.

In the Transmit direction, the MAC Transmit Function Sublayer (TFUN) module of the MAC core generates input byte data streams in response to frame byte streams supplied by the host system. The ARGMMII module takes this data and outputs 4-bit wide data at the frequency of the RGMII reference clock.

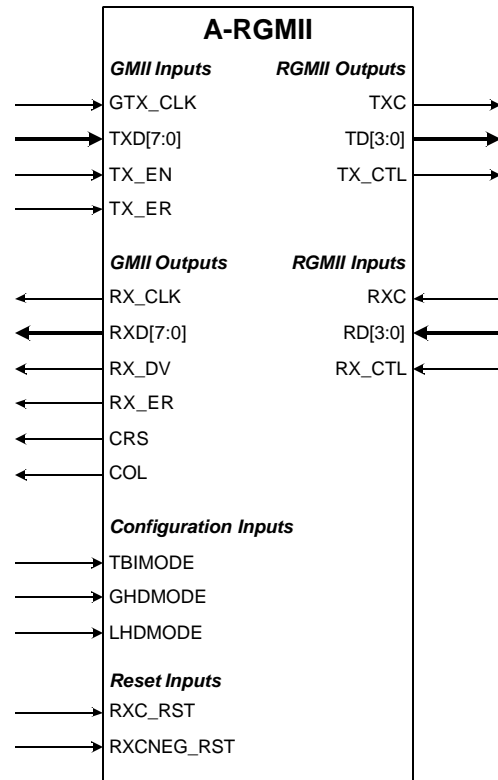
In the Receive direction, the RGMII PHY provides 4-bit data synchronous to the RGMII reference clock. The ARGMMII module first detects the Start-of-Frame Delimiter (SFD) in order to ensure the proper nibble boundary, and then outputs the SFD followed by the frame to the Receive Function module via the GMII/MII/TBI interface.

Tool Flow

The supplied testbenches have been run on different simulator software and different platforms before shipment in order to ensure correct operation at the licensee's facility. Among the tools used were: Cadence Verilog NC (native compile), Cadence Verilog (cross compile), and Model Technology's ModelSim. The code has been run in both Unix and PC environments.

In addition, the Verilog RTL has been constrained and synthesized by Synopsys Design Compiler using third party standard cell libraries. The libraries were selected to be representative of the current technology at the time of testing. The constraints and design rules used during this process are intended to be generic in nature.

Block Instantiation Diagram



Implementation

The combined system of the MAC core with the A-RGMII interface exports the transmit and receive packet streams directly to the top of the design, thereby allowing customer-specific DMA solutions to be readily connected to the core. This in turn allows the MAC's performance to be tailored to and optimized for each individual application.

The Host interface needs to be tailored to the individual application. Where the MAC is used in a multi-port device like a switch, the Host CPU interface will typically be to an embedded processor. In an end-station implementation, the interface might be to the end-station bus.

Reference Technology Gate Count: approx. 1000

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