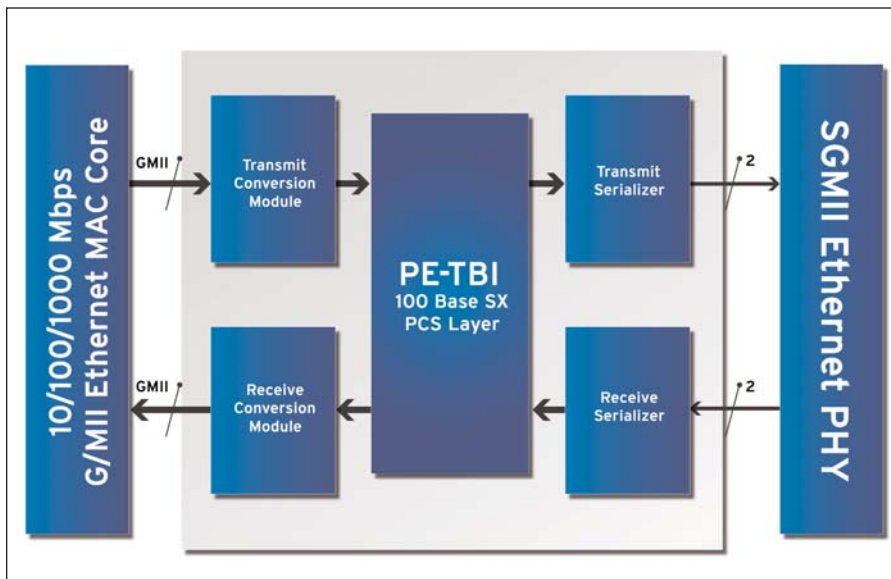


Ethernet IP

Serial Gigabit Media Independent Interface

M-SGMII

D A T A S H E E T



M-SGMII submodules and data flow.

Mentor's Serial Gigabit Ethernet Solution

The Mentor Graphics® M-SGMII module provides a serial gigabit media independent interface that facilitates connection between any IEEE 802.3 standard GMI or MII interface and a SGMII interface which is compliant with version 1.7 of the Serial-GMII specification.

The M-SGMII offers a single, generic reduced pin-count interface for all Ethernet Media Access Controllers (MAC) speeds and duplex modes which are typically found at the network edge. The M-SGMII allows devices such as the PE-MCXMAC 10/100/1000Mbps Ethernet MAC to connect to reduced pin-count PHYs.

The M-SGMII uses Mentor's silicon-proven 1000 base SX PCS layer soft core (PE-TBI) to provide the 8B/10B encoding, decoding, and auto-negotiation functionality defined in Clause 36 of IEEE 802.3z specification. This allows link partners to synchronize to each other and exchange information regarding their configuration capabilities using a symbol stream that is a proven industry standard. The M-SGMII also instantiates transmit and receive conversion and rate adaptation modules that allow for G/MII data/control conversion, half duplex control encoding, and clock domain interfacing to the SGMII clock domain. The M-SGMII core includes optional modules for 10-bit comma alignment and a process independent (soft core) generic Serializer/Deserializer (SerDes) block.

Major product features:

- Converts 802.3 GMII interface into a Serial Gigabit link for reduced pin count applications
- Supports version 1.7 of the Serial-GMII specification
- Supports 10/100/1000Mbps Ethernet MAC operating speeds
- Separate layer of hierarchy for high speed clocks
- Includes fully synthesizable soft SerDes modules for process independent applications
- Optional support for 10-bit parallel based 3rd party SerDes
- Optional 10-bit comma alignment support

Deliverables:

- RTL source code
- Wrapper files for 10/100/1000Mbps Ethernet MAC (PE-MCXMAC) integration
- Synthesis constraints files
- Verilog functional verification suite
- Full design, verification, and revision documentation

Related products:

- **PE-MCXMAC** - 10/100/1000 Mbps Ethernet MAC-A-MCXFIF
- **A-MCXFIF** - 10/100/1000Mbps FIFO module

Functional Overview:

The M-SGMII uses two data signals and two clock signals to communicate, transmit, and receive encoded data and link information between the Ethernet MAC and a SGMII Ethernet PHY. The M-SGMII performs this communication at Gigabit SerDes speeds, requiring a 625 MHz DDR clocking scheme.

Both the transmit and receive paths leverage the physical coding sublayer and the auto-negotiation sublayers of the IEEE 802.3z specification, as contained in Clauses 36 and 37. In the transmit direction, the 10-bit encoded data is serialized and output over the interface. In the receive direction, the single-bit input is made parallel after being aligned to comma characters and recovering the clocks performs all of the clocks.

Block Interface Signals

Signal	Type	Description
MSTRRST	Input	Master Reset Signal
RESET_BYPASS	Input	SCAN Testing Reset Bypass
MSGMII_SPEED[1:0]	Input	G/MII Ethernet Speed
G/MII Interface Signals		
TX_CLKI	Input	G/MII Transmit Clock
TXD[7:0]	Input	G/MII Transmit Data
TX_EN	Input	G/MII Transmit Enable
TX_ER	Input	G/MII Transmit Error
RX_CLKI	Input	G/MII Receive Clock
RXD[7:0]	Output	G/MII Receive Data
RX_DV	Output	G/MII Receive Data Valid
RX_ER	Output	G/MII Receive Error
COLL	Output	G/MII Collision Indicator
CRS	Output	G/MII Carrier Sense
SGMII Interface Signals		
TXCLK	Input	SGMII Serial Transmit Clock
TX	Output	SGMII Serial Transmit Data
RXCLK	Input	SGMII Serial Receive Clock
RX	Input	SGMII Serial Receive Data
Clocking Tree Signals		
PMA_RXCLK0o	Output	PMA Receive Clock 0 output
PMA_RXCLK1o	Output	PMA Receive Clock 1 output
PMA_RXCLK0	Input	PMA Receive Clock 0, 62.5MHz
PMA_RXCLK1	Input	PMA Receive Clock 1, 62.5MHz
GTX_CLKI	Input	Gigabit Transmit Clock, 125MHz
TXCLKX2	Input	SGMII Serial Transmit Clock x2
MII Management Interface Signals		
MDI	Input	MIIM Serial Data In
MDL_PAD	Input	MIIM Serial Data In from Pad
MDC	Output	MIIM Clock
MDO	Output	MIIM Serial Data Out
MDOE	Output	MIIM Output Data Enable

For complete clock domain isolation of the M-SGMII from the MAC, both transmit and receive elasticity FIFOs are used at the G/MII interface. Note that clock domain isolation FIFOs can cause limitations on the maximum frame sizes under worst-case clock conditions. However, there are no issues for IEEE-compliant frame sizes.

The M-SGMII core also includes support for MAC speeds less than Gigabit rates. In order to maintain a constant clock frequency at the PHY interface for all MAC speeds, the MII bus data is replicated internally to maintain a Gigabit rate at the output of the M-SGMII core.

Nibble packet data transmitted by a 100Mbps MAC is aligned, concatenated, and replicated 10 times. Nibble packet data transmitted by a 10Mbps MAC is aligned, concatenated, and replicated 100 times. Packet data received by the M-SGMII via the PHY must be undersampled by a factor of 10 before being sent to a 100Mbps MAC. Packet data received by the M-SGMII via the PHY must be undersampled by a factor of 100 before being sent to a 10Mbps MAC.

For half-duplex functionality, carrier sense is inferred from rx_dv, and collision is derived from the simultaneous assertion of tx_en and rx_dv. application.

Reference Technology Gate Count:

- 18,000 gates

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