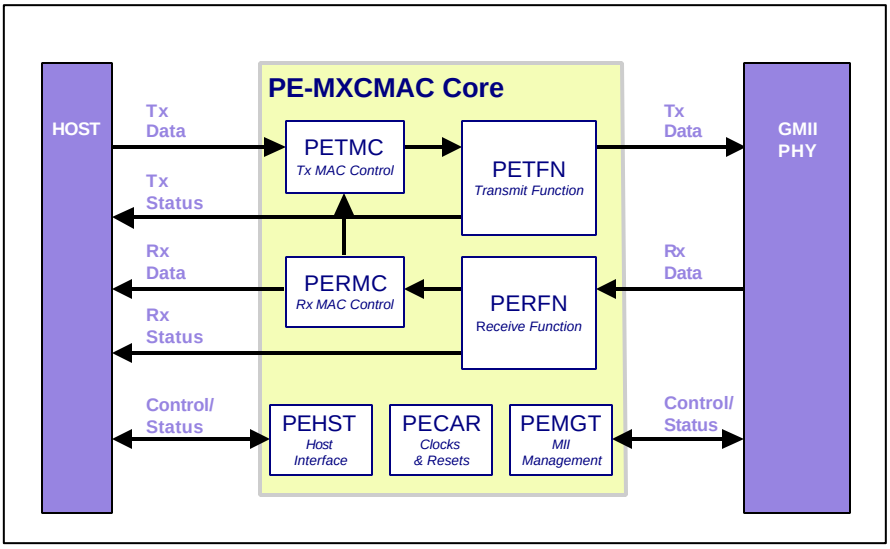
PE-MCXMAC™
Triple-Speed Ethernet MAC

Inventra™ Soft Core (RTL IP)

D A T A S H E E T



PE-MCXMAC Block Diagram

Overview

The PE-MCXMAC™ provides a 10/100/1000 Mbps Ethernet Media Access Controller (MAC) with a GMII Gigabit Media Independent Interface for incorporation in a customer's own ASIC design.

The inclusion of a GMII means that several alternative PHY interfaces are readily supported, including 10/100 Mbps Reduced MII, 10/100 Mbps Serial MII, Reduced GMII, Serial GMII and 1000 Mbps TBI SERDES (all also available in the Mentor Graphics Inventra™ range of soft cores).

The PE-MCXMAC also includes the MAC Control sublayer, which provides support for Control frames, particularly PAUSE frames. (Other types of Control frames can be supported through setting optional configuration bits.) Both Symmetric and Asymmetric Flow Control are supported.

There are many different possible applications for the PE-MCXMAC, including network interface designs, Ethernet switching designs, and test equipment designs.

The PE-MCXMAC module was designed in Verilog. The design may be synthesized in .25µm CMOS (or better).

Major Product Features:

- Operates at 10, 100 or 1000 Mbps
- Meets IEEE 802.3, 802.3u, 802.3x, 802.3z and 802.3ac specifications
- Supports 802.3x Full Duplex Flow Control; also supports Half Duplex when operating at 10 or 100 Mbps (with Back Pressure)
- 8-bit MAC engine, optimized for size and minimal latency
- Built-in MII/GMII interface
- Optional interface modules available for RMII, SMII, RGMII, SGMII and TBI SERDES
- 32-bit CPU interface
- Built-in MII management with suppressed preamble, sequential cycle and variable clock features
- Generates 52-bit Transmit & 33-bit Receive statistics vectors, supporting RMON and SNMP
- Additional PE-MSTAT register-based statistics module available
- Fully synthesizable
- Scan insertion-friendly design

Deliverables:

- Verilog source code
- Synthesis constraints files
- Functional testbench
- Expanded Statistics vectors for certain RMON and Etherstats applications

Mentor Graphics is the leading supplier of a broad range of IP soft cores targeting standards-based communications applications. These highly re-usable cores help systems and chip designers get to market faster.

Structure

The PE-MCXMAC module consists of seven sub-modules:

PETFN Transmit Function: The PETFN module accepts frames from the system transmit interface, and prepends a 7-byte preamble and Start of Frame Delimitor. PETFN waits the pre-programmed Inter-Packet Gap before outputting the preamable. Transmission errors are signaled via the TX_ER signal.

PETMC Transmit MAC Control: The PETMC module is responsible for the multiplexing of normal Transmit frames and Control frame requests by the system. It provides native support for PAUSE Flow Control frames.

PERFN Receive Function: The PERFN module accepts packets via the GMII, extracts frames, and strips off the preamble and Start of Frame Delimitor from each frame before presenting them to the system. It also calculates the CRC of the received frame for checking against the Frame Check Sequence field. Valid data is qualified by RX_DV.

PERMC Receive MAC Control: The PERMC module is responsible for detecting Control frames in the Receive data stream. Each frame is examined to determine if it is a Control frame and if so, whether it is a PAUSE frame.

PEHST Host Interface: This 32-bit wide interface gives the external host processor access to the range of status and control registers included in the PE-MCXMAC.

PECAR Clocks & Resets: For ease of scan and buffer insertion, all the clock and reset circuitry is located in a single module. Stubs are provided for connection to clock trees. The PECAR module also allows the normal reset logic to be bypassed for scan chain insertion.

PEMGT MII Management: The PEMGT module drives the MII Management Interface across which control and status information is exchanged with the attached PHY. It provides an interface between the host processor and one or more PHYs.

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Transmit Operation

The system interface presents transmit frames to the PE-MCXMAC. These frames do not need to be padded etc. in advance. Where set in the configuration registers or through per-packet overrides, the PE-MCXMAC may pad the frame and/or append a valid Frame Check Sequence. A Transmit statistics vector is output with each packet transmission (or abortion) for external statistics collection.

In 1000 Mbps operation, 8 bits of packet data are output per clock. At speeds less than 1000 Mbps, 4 bits of packet data are output per clock.

Receive Operation

The external PHY device presents receive packets to the PE-MCXMAC. The PE-MCXMC scans the preamble looking for the Start of Frame Delimiter (SFD): when found, the preamble and the SFD are stripped out and the frame is passed to the system. A Receive statistics vector is also output for frame filtering and statistics collection.

The PE-MCXMAC also outputs 9 bits of the data CRC for use in the kind of filtering commonly implemented in Network Interface Card (NIC) applications.

Implementation

The PE-MCXMAC exports the transmit and receive packet streams directly to the top of the design, thereby allowing customer-specific DMA solutions to be readily connected to the core. This in turn allows the core's performance to be tailored to and optimized for each individual application.

The PE-MCXMAC module comes with a standard GMII interface. However, due to market demands for additional interfaces, five optional PHY interfaces are also offered:

- PE-SMII (Serial Media Independent Interface)
- PE-RMII (Reduced Media Independent Interface)
- A-RGMII (Reduced Gigabit Media Independent Interface)
- M-SGMII (Serial Gigabit Independent Interface), and
- PE-TBI (Ten-Bit SERDES Interface).

Reference Technology Gate Count: 15000

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