A P P N O T E S SM

Using the PE-MACMII as a Building Block in System Design

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Introduction

Mentor Graphics Ethernet Modules are Building Blocks that help systems and chip designers get products to market faster. Each Module contains the key functions required to implement a major system component. Each Module is written in Verilog and may contain several sub-modules. By combining these sub-modules and adding any additional required functions, customers may create ASIC designs in less time and with less risk than creating the work from scratch.

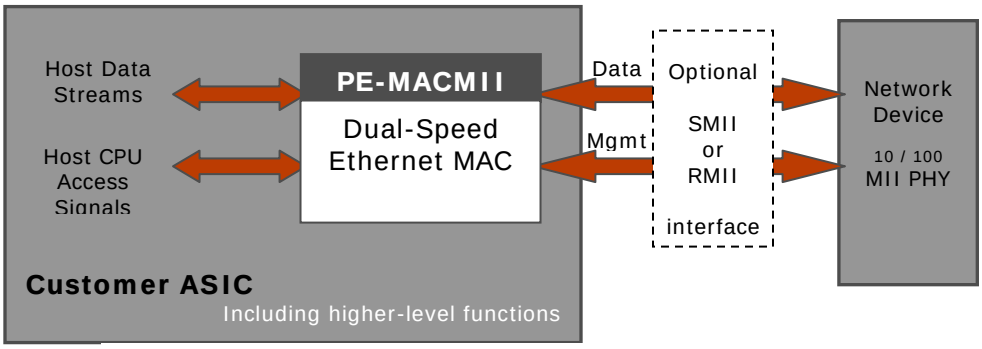


Figure 1 – Module Block Diagram

The PE-MACMII module may be used in many different applications.

The PE-MACMII module has been optimized for applications using ***multiple*** Ethernet MACs such as switches, multi-port bridges, embedded applications and routers

PE-MACMII – Sub Modules

The PE-MACMII™ is a Module that may be incorporated in a customer's own ASIC design. The PE-MACMII module consists of six sub-modules. These sub-modules are the transmit and receive portions of the Ethernet MAC controller plus three supporting sub-modules. These sub-modules, together with additional modules may be connected together to make a dual speed (100 Mbps and 10 Mbps) Ethernet controller. There are many different possible applications, including network interface designs, Ethernet switching designs, and test equipment designs.

The PE-MACMII module was designed in Verilog. The nominal module size is approximately 12,000 gates. The design may be synthesized in .5 micron CMOS (or better).

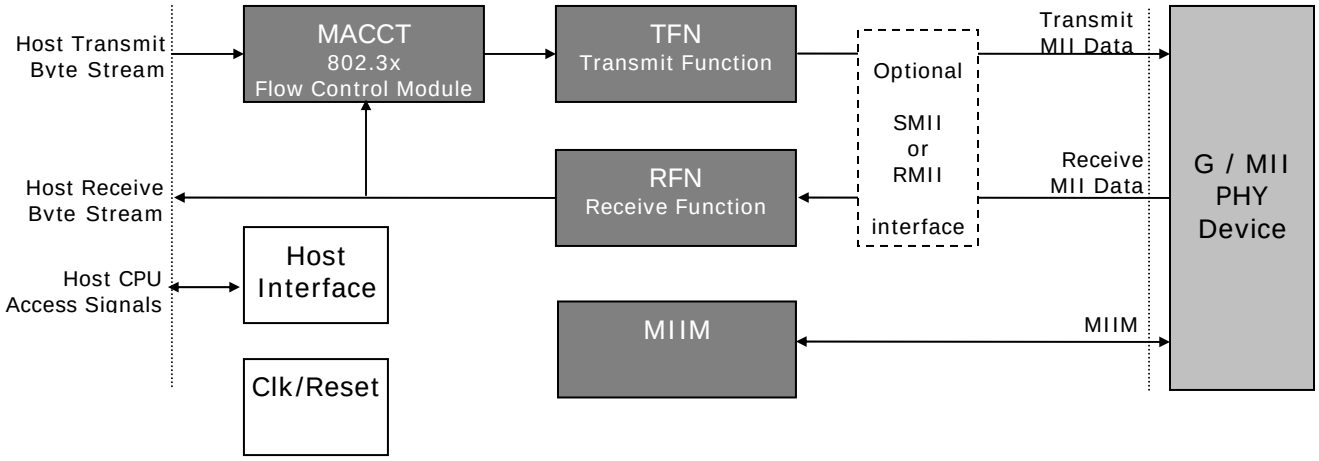


Figure 2 – Layout of the PE-MCXMAC Module

Figure two shows that the PE-MACMII module consists of six sub-modules. The six modules can be thought of as two groups. These are the MAC functions and the supporting network I/O functions. The MAC functions are contained in the transmit and receive modules TFUN and RFUN. These modules must be included in every implementation. The 802.3x PAUSE frame function is implemented by the MACCTL module.

If the PE-MACMII module is used to create a multi-port device like a switch, the Host CPU interface will typically be to the embedded processor. In the case of an end-station implementation, this might be the end-station bus. The Host interface needs to be created for the individual application.

Management Statistics

The PE-MACMII transmit and receive functions are not instrumented with large numbers of counters for statistics collection. A vector-generation method is used instead. The vector technique has the effect of simplifying the timing of many asynchronous events.

The vector method is also more efficient in multiple-MAC systems. Statistics accumulation may be done centrally for all of the MACs in the system, reducing gate count and improving processing efficiency. A result of this approach is that the statistics gathering mechanism must be created outside the MAC on a case-by-case basis.

Statistics Gathering and Vectors

Most activity in a MAC is centered on major events such as completion of packet reception or completion of packet transmission attempts. When these major events occur, the PE-MACMII module generates a statistics vector, summarizing the detailed results associated with the event. The vector is then latched into a statistics collection block. A vector is latched once for each major event.

This vector approach reduces the requirement for individual synchronization of many individual events. The approach also reduces the gate count by eliminating the need for flip-flops scattered around the MAC design.

When multiple-MAC designs are involved, the statistics-collecting block may be common for all MACs. Again, the vector approach reduces the complexity of the design and the gate count. Central statistics gathering is also easier than distributed gathering when it comes to parsing cumulative and derivative statistics.

There are generally two different vectors, one for receive and one for transmit. Vectors may be designed to include or exclude as many different parameters as a customer requires. Examples of vectors and parameters are shown in Figure eight.

Statistics Gathering and Vectors Example

In this implementation example, the transmit vector is fifty-two bits long and the receive vector is thirty-one bits long. Vector implementations are not limited to these parameters or lengths

Transmit Status Bit		Receive Status Bit	
Bit	Meaning	Bit	Meaning
51	Transmit back pressure previous packet		
50	Transmit previously paused		
49	Transmit pause control frame		
48	Transmit control frame	30	Receive VLAN tag detected
47-32	Total bytes transmitted on wire	29	Receive unsupported opcode
31	Transmit under run	28	Receive pause frame statistics
30	Transmit giant	27	Receive control frame statistics
29	Transmit late collision	26	Dribble nibble
28	Transmit excessive collision	25	Broadcast packet
27	Transmit excessive defer	24	Multicast packet
26	Transmit packet defer	23	Receive OK
25	Transmit broadcast	22	Field length out of range
24	Transmit multicast	21	Field length check error
23	Transmit done	20	CRC error
22	Transmit field length out of range	19	Receive code violation
21	Transmit field length check error	18	Carrier event previously seen
20	Transmit CRC error	17	RXDV event previously seen
19-16	Transmit collision byte count	16	Packet ignored
15-0	Transmit byte count	15-0	Received byte count

Application: Common Examples

The PE-MACMII module may be used in many different applications. However, it has been optimized for applications using multiple Ethernet MACs such as

- switches
- multi-port bridges
- routers

Application: PE-MACMII core as a switch building block

The PE-MACMII module has been optimized for use in multiple-MAC applications. These include switches, multi-port interface cards, and routers. Figure three shows a typical application where the PE-MACMII is used as a building block for an eight-port switch.

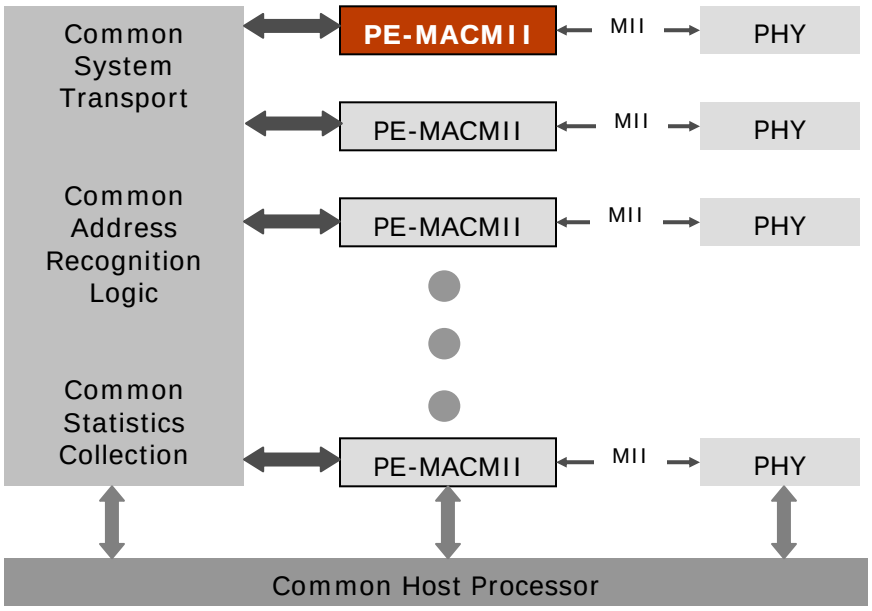


Figure 4 – PE-MACMII Module used in an 8-port Ethernet Switch

The exact nature of the common sections for system data transport, address recognition, and statistics will be application dependent. The PE-MACMII module has enough built-in flexibility to cover almost any system concept.

The PHY devices may be internal to the design or external; with an internal PHY, the MII might be only a logical implementation without line driving capability; and the ports may be dual-speed or fixed at one speed. The PE-MACMII is capable of being adapted to each of these variations in design.

Application: PE-MACMII core as a network interface controller

The example below shows the PE-MACMII module implemented in a network controller chip. The chip is used to create a PCI-based network controller for PCs.

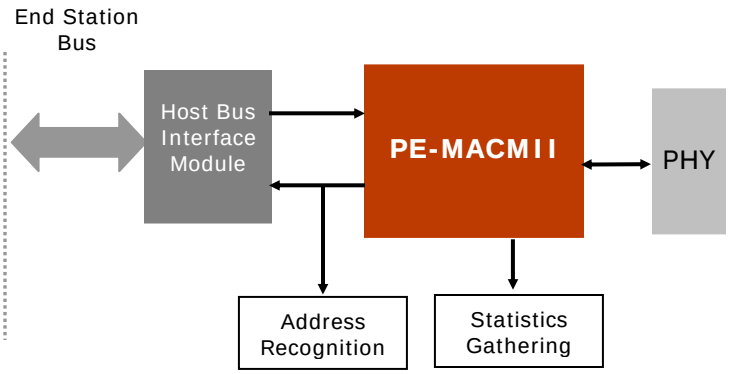


Figure 5 – Single MAC implementation

Management statistics are generated as vectors by the PE-MACMII. A mechanism must be created to collect these vectors and parse the information appropriately.

The generalized byte streams of data may be interfaced to any bus type. Depending on the sophistication and the bus, the bus interface module might range from a trivial to a very complex implementation. The PE-MACMII module can be implemented with PCI-express, PCI, MCA, VLB, S-Bus, Nubus, SCSI, Multibus, and many more.

Host Interface Options

The PE-MACMII module connects to a host system. The host system may be of different types. In a switch system, the host will generally be the embedded CPU or the backplane switching fabric. In a network interface card, the host might be a general-purpose computer communicating over the computer bus through a VXI, FMC, PCI or PCI-express interface.

Optional Interface Modules

The PE-MACMII module comes with a standard MII interface. However, due to market demands for additional interfaces, we offer four optional PHY interfaces as separate modules. These optional interfaces are the PE-SMII (Serial Media Independent Interface), the PE-RMII (Reduced Media Independent Interface), the PE-ENDEC (10T Interface), and the PE-PMD (100X Interface).
These interface modules are noted in figure six below.

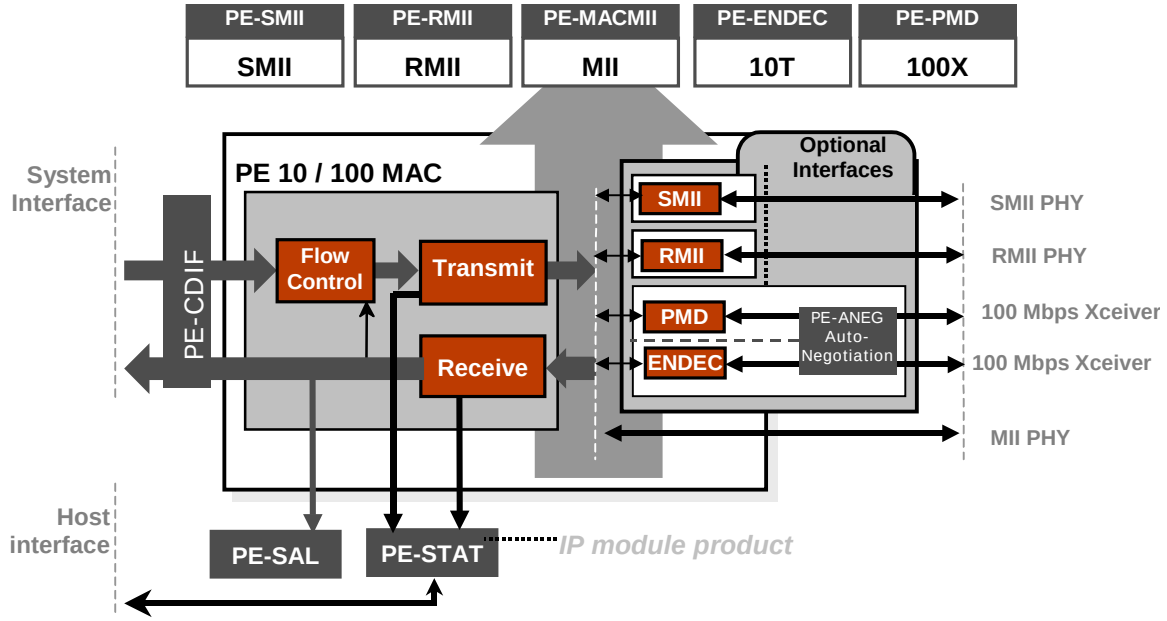


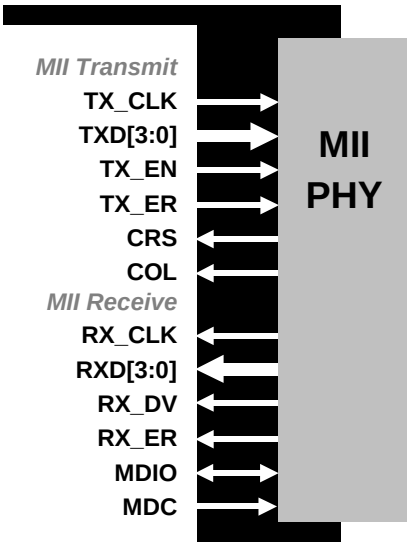
Figure 6 – 10 / 100 Mbps Ethernet family of Cores

The MII Interface

The PE-MCXMAC core communicates with external PHY devices through the logical G / MII interface. The logical G / MII is divided into two signal sets. One set handles data transmission and reception while the second set handles G / MII management functions.

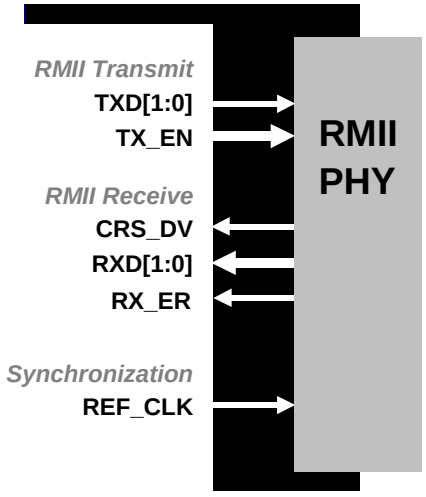
The G / MII interface is the industry standard interface method for connecting MACs with PHY chips. IEEE 802.3u Clause 22 and IEEE 802.3z Clause 35 define this interface.

A pair of signals (MDC / MDIO) are defined for the MII as a management interface. This management interface is used to access the PHY's registers for initialization and auto-negotiation activities. The management interface is able to address up to 31 PHY's. Therefore, in multiple MAC / PHY designs, each MAC chip only requires one pair of these signals.



Optional PE-RMII Interface

The PE-RMII is a module that combines with modules from our PE-MACMII product to furnish a Media Access Controller that provides a PHY interface that requires six signal pins rather than the sixteen signal pins of a standard MII interface.



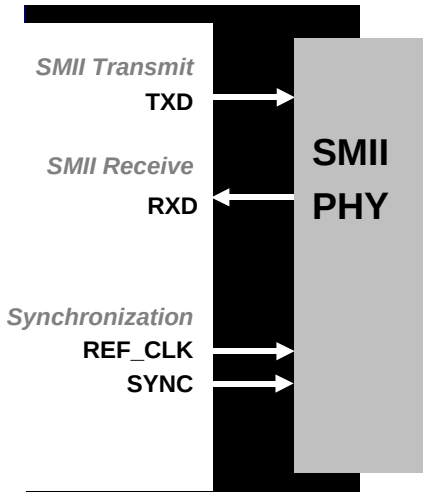
Although the RMII interface is not an IEEE standard, it is supported through the RMII Consortium and is receiving broad industry support from PHY vendors. The RMII interface provides a low pin count alternative to the IEEE MII interface.

The RMII interface performs the conversion from the 2.5 / 25 MHz nibble-wide MII interface to a 50 MHz di-bit (two-bit) interface. It provides independent di-bit transmit and receive data paths.

The PE-RMII is useful in designs where multiple MACs are interfacing to external PHY's. The RMII interface provides for a single 50 MHz clock per PHY chip. The two-wire management interface for RMII (MDIO / MDC) is identical to MII.

Optional PE-SMII Interface

The PE-SMII is a module that combines with modules from the Alcatel PE-MACMII product to furnish a Media Access Controller that provides a PHY interface that requires two signal pins rather than the sixteen signal pins of a standard MII interface, or the six pins of an RMII interface.



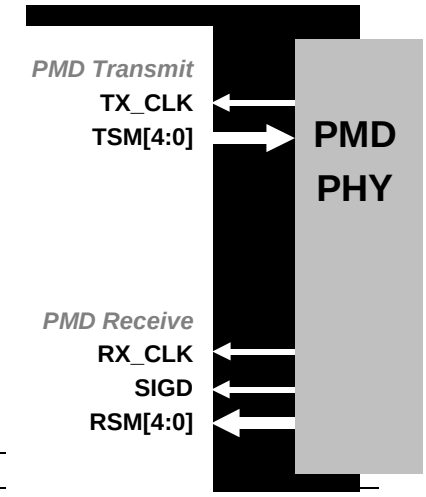
Although the SMII interface is not an IEEE standard, it is receiving industry support from PHY and system vendors. The SMII interface provides a low pin count alternative to the IEEE MII interface.

The SMII interface performs the conversion from the 2.5 / 25 MHz nibble-wide MII interface to a 125 MHz single-bit interface. It provides independent single-bit transmit and receive data paths.

The PE-SMII is useful in designs where multiple MACs are interfacing to external PHY's. The SMII interface provides for a single 125 MHz clock and one sync signal per PHY chip. The two-wire management interface for SMII (MDIO / MDC) is identical to MII.

Optional PE-PMD interface

The PE-PMD is a module that combines with modules from our PE-MACMII product to furnish a Media Access Controller for use in designs with the five-bit TP-PMD interface as specified in IEEE 802.3u Clause 24.2.2.

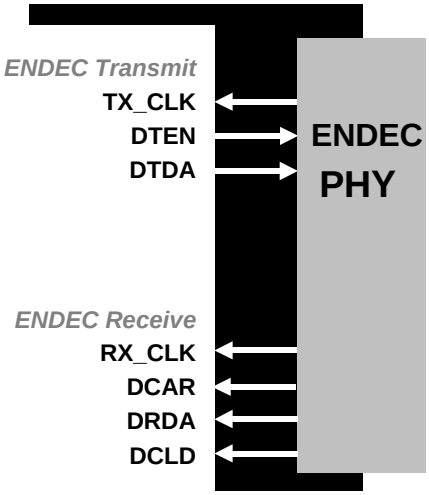


This module provides the 4B / 5B encoding / decoding circuitry in the PCS. It performs ciphering and deciphering with the included self-synchronizing descrambler. It also contains the 330ms link fail timer. This circuitry is useful, for example, for the design of digital 10 / 100 PHY's.

Optional PE-ENDEC interface

The PE-ENDEC is a module that combines with modules from the Alcatel PE-MACMII product to furnish a Media Access Controller for use in designs with a PHY interface that conforms to a seven-wire interface, Serial Network Interface (SNI), or a General Purpose Serial Interface (GPSI).

The module converts the 10Base-T MII transmit nibble stream into the serial bit stream for a Manchester Encoder and converts the receive ENDEC 10base-T serial bit stream from a Manchester Decoder into the 10Base-T MII nibble stream. Loss of Carrier error detect, signal_quality_error monitoring, and the jabber protection function are also included. This circuitry is useful for designs interfacing to a seven-wire interface as well as the design of digital 10 / 100 PHY's.



CMOS Device Utilization

The PE-MACMII module was designed in Verilog. The nominal module size is approximately 12,000 gates. The design may be synthesized in .5 micron CMOS (or better). This core technology was originally shipped in 1995, and continues to be utilized to this day.

Xilinx Device Utilization – ISE Historical Data

The following table shows estimated device utilization for the PE-MACMII core in Xilinx parts.

Device Family[1]	Speed Grade	Utilization[2]			Performance (f_{MAX})[3]
		CLB Slices	RAM Blocks	I/O Count	
Virtex II	-4	1035	0	223	61MHz
Spartan II	-5	1029	0	223	44MHz

Notes:

1. The PE-MACMII was successfully compiled in at least one device of the device family listed. While not all devices in the device family will be able to meet the timing and utilization requirements, the PE-MACMII will be usable in more than one device of each family.

2. The CLB and RAM block count listed is using FPGA Express and Xilinx's Foundation ISE 3.3i software. Other logic synthesizers and different versions of Foundation may yield different results. The I/O count assumes all the core signals are routed to I/O pins on the part. Usually customer designs will incorporate many of these signals internally in the device.

3. An F_{MAX} of 25MHz is all that is required to meet the IEEE 802.3 specification for 100Mbps operating mode, the actual F_{MAX} achieved will vary with logic placement.

Altera Device Utilization – Quartus Historical Data

The following table shows estimated device utilization for the PE-MACMII core in Altera parts.

Estimated Device Utilization for the PE-MACMII						
Device Family[1]	**Speed Grade**	**Utilization[2]**			**Performance (f_{MAX})[3]**	**Global Resources**
		Logic Cells	**EABs / ESBs**	**I/O Count**		
APEX 20KE	-1	1784	0	223	25MHz	7 global signals used
APEX 20K[4]	-1	1787	0	223	25MHz	7 global signals used
FLEX 10KE[4]	-1	2296	0	223	25MHz	6 global signals used
ACEX 1K[4]	-1	2291	0	223	25MHz	6 global signals used

Notes:

1. The PE-MACMII was successfully compiled in at least one device of the device family listed. While not all devices in the device family will be able to meet the timing and utilization requirements, the PE-MACMII will be usable in more than one device of each family.
2. The logic cell and EAB/ESB count listed is using Altera's OEM version of Leonardo Spectrum v1999.1j Level 1 and Quartus 2000.09 or MAX+PLUS II v10.0. Other logic synthesizers and different versions of Quartus or MAX+PLUS II may yield different results. The I/O count assumes all the core signals are routed to I/O pins on the part. Usually customer designs will incorporate many of these signals internally in the device.
3. An F_{MAX} of 25MHz is all that is required to meet the IEEE 802.3 specification for 100Mbps operating mode, the actual F_{MAX} achieved will generally be higher. The PE-MACMII successfully meets timing in the device family according to the Altera software, but to date a post layout netlist has not been run against the PE-MACMII testbench to check for possible timing violations.

Spartan-6 Four Port System – with Precision Synthesis

This example speaks to using the PE-MACMII in a 4-port Ethernet application implemented in a Xilinx Spartan-6 device.

The preferred device is a XC6SLX45 Speed Grade 3.

The device advertises the following salient features:

- CLB Slices – 6,822
- Max User I/O – 358 pins

The PE-MACMII was designed with multiple core systems in mind. The XC6SLX45 has adequate logic resources for the given system of 4 Ethernet MACs. The considerations regarding utilization of the Common Host, Clocking, and PHY I/O resources are given in a seperate paragraph, below. Given the stated considerations, the PE-MACMII is a great choice for this design.

A generic block diagram of the Ethernet portion of the entire design should look very similar to the following figure:

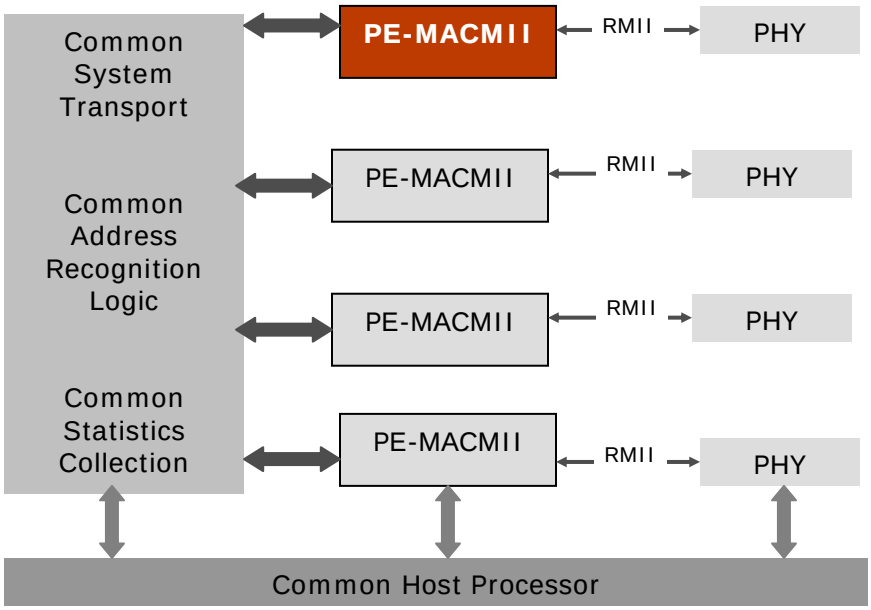


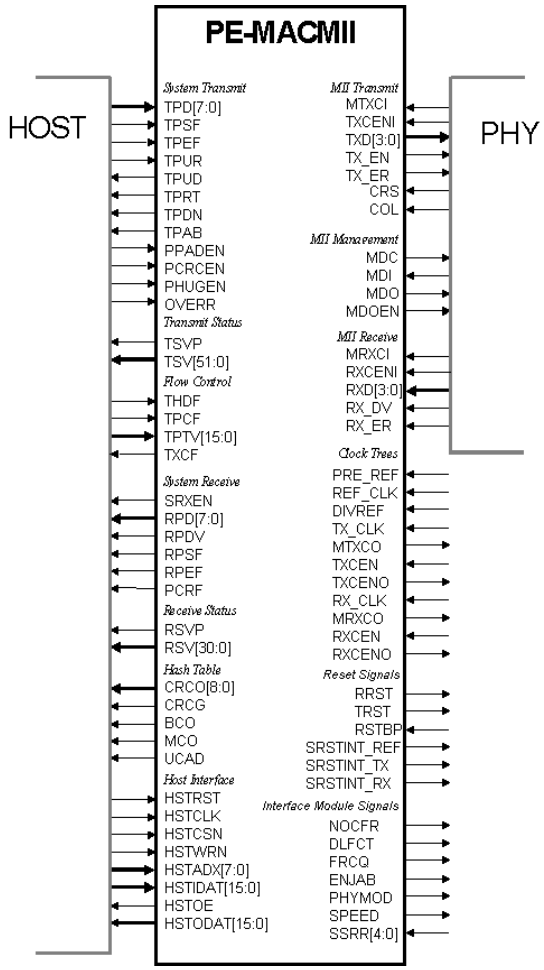
Figure 11 – PE-MACMII Module used in an 4-port Ethernet Application

Xilinx Spartan-6LX45 – Host, PHY and Clock connections

HOST - This example assumes that the common transport, statistics and address logic is implemented within the FPGA. Therefore, all the PE-MACMII "host" signals are used internally to the system and are not tied to FPGA i/o pins.

PHY – The PHY connection will consume some of the 345 i/o pins available on the XC6SLX45. The standard MII will take 16 pins per phy, or 64 pins total for the 4 MAC system design. The Reduced MII interface will take 6 pins per phy, or 24 pins total for the 4 MAC system design.

Clock – This example assumes that the clock pins for all 4 PE-MACMII are driven by the same Spartan-6 clock resources. Therefore the clock inputs don't need to be reduntant.



Xilinx Device Utilization – Precision Synthesis

The following table shows estimated device utilization for the PE-MACMII core in Xilinx parts.

Device Family[1]	Speed Grade	Utilization[2]			Performance (f_{MAX})[3]
		CLB Slices	RAM Blocks	I/O Count	
Spartan VI	-3	300	0	223	25

Notes:

1. The PE-MACMII was successfully compiled in at least one device of the device family listed. While not all devices in the device family will be able to meet the timing and utilization requirements, the PE-MACMII will be usable in more than one device of each family.

2. The CLB and RAM block count listed is using Precision Synthesis and Xilinx's Foundation ISE 11.1 software. Other logic synthesizers and different versions of Foundation may yield different results. The I/O count assumes all the core signals are routed to I/O pins on the part. Usually customer designs will incorporate many of these signals internally in the device.

3. An F_{MAX} of 25MHz is all that is required to meet the IEEE 802.3 specification for 100Mbps operating mode, the actual F_{MAX} achieved will vary with logic placement.

Conclusion: PE-MACMII and Precision Synthesis are a Winning Combination

A single PE-MACMII uses 300 CLBs per core, for a total of 1,200 CLB's for a 4 core design. This represents only 17.59% of the 6822 CLBs available in the XC6SLX45.

The combination of the Mentor Graphics PE-MACMII and Precision Synthesis allow a system designer to implement multiple Ethernet Media Access Controllers in a cost effective, efficent design utilizing state of the art Xilinx Spartan-6 FPGAs.

References

[1] IEEE Std. 802.3, CSMA/CD Access Method and Physical Layer Specifications, Copyright Institute of Electrical and Electronic Engineers, Inc., 1993
[2] IEEE Std. 802.3u, MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100 Mb/s Operation (Supplement to IEEE 802.3), Copyright Institute of Electrical and Electronic Engineers, Inc., 1995.
[3] ISO11801, Copyright International Organization for Standards, 1995