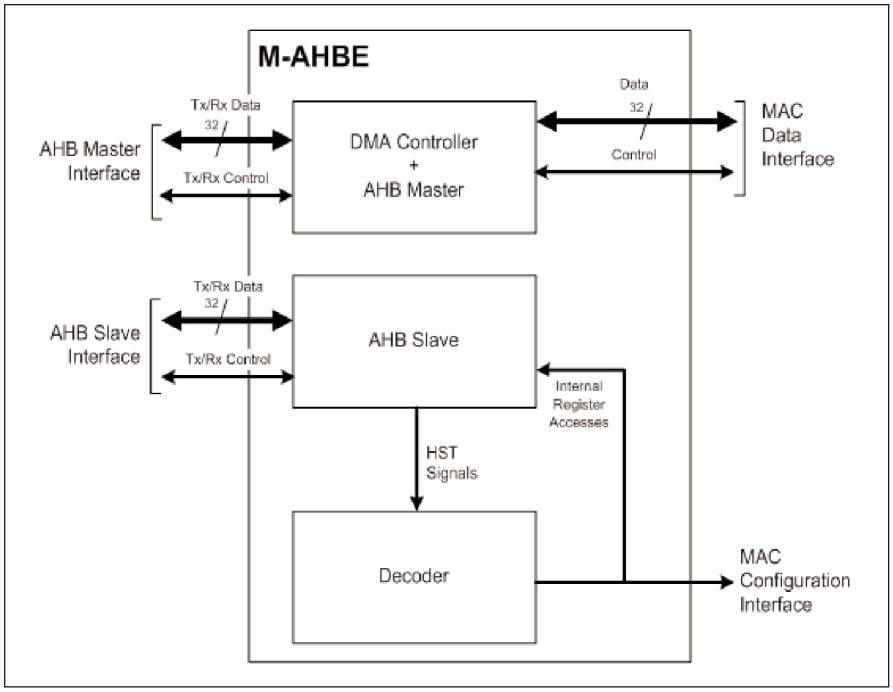
Ethernet IP

AHB DMA Ethernet Bridge

M-AHBE

D A T A S H E E T



M-AHBE sub-modules and data flow

Overview

The M-AHBE™ module from Mentor Graphics provides a DMA bridge between a host system that uses an AMBA AHB™ bus and Ethernet MACs available in the Mentor Graphics Ethernet IP library. Use of the M-AHBE module also requires the use of a suitable FIFO alongside the Ethernet MAC.

The M-AHBE module interfaces to the host system through 32-bit AHB master and slave ports. On the MAC side of the module, it has a high-performance synchronous interface for DMA data transfer to/from the FIFO and a semi-synchronous interface for configuring the MAC and the FIFO through their HST interfaces.

For ease of handling by software, transfers are handled using linked lists of transfer descriptors, which together define one buffer in host memory for Tx operations and another for Rx operations. These buffers will typically be configured as ring buffers, but this is up to the user to implement.

Registers within the M-AHBE provide control and status information concerning these transfers. The registers are accessed through the AHB slave port, alongside accesses to the HST interfaces on the MAC and the FIFO.

The M-AHBE module was designed in Verilog and is provided to licensees with a behavioral testbench.

Major product features:

- AMBA AHB 2.0 compliant master port for payload data transfer
- AMBA AHB 2.0 compliant slave port for DMA bridge, FIFO, and MAC configuration
- Synchronous backend interface compatible with Mentor Graphics PE-MCXMAC and PE-MACMII Ethernet MAC cores and associated FIFO modules
- Asynchronous interface included for addition of Mentor Graphics PE-MSTAT statistics module
- RAM-free synchronous single-clock domain design
- 32-bit architecture
- Linked-list transfer descriptors for minimal software overhead
- Speed of operation is synthesis dependent only
- Supports ASIC and FPGA based designs

Deliverables:

- Verilog source code
- Detailed design documentation
- Synthesis constraints files
- Functional stand alone and integrated testbenches with documentation
- Wrapper integrating the M-AHBE with Mentor's PE-MCXMAC or PE-MACMII cores

Related products:

- PE-MCXMAC™ 10/100/1000Mbps Ethernet MAC core
- A-MCXFIF™ 10/100/1000Mbps FIFO module
- PE-MACMII™ 10/100Mbps Ethernet MAC core
- M-MIIFIF™ 10/100Mbps FIFO module

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Structure

The M-AHBE pack includes the following RTL modules:

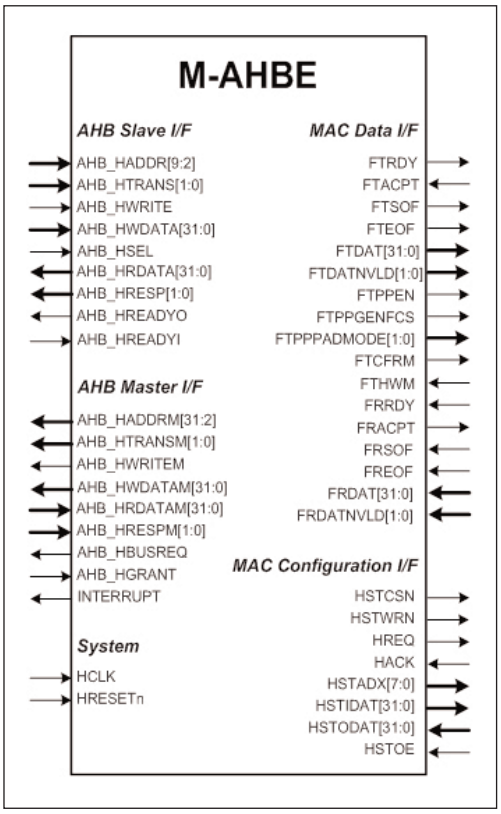
- **MAHBE** – *Top-level module*
- **DMA** – *Includes logic for the AHB master interface and contains the DMA controller*
- **SLAVE** – *Includes logic for the AHB slave interface*
- **DECODER** – *Address decoder module*

Functionality

The M-AHBE includes a single DMA controller which is used both for transmit operations and for receive operations. (Where both channels compete for the use of the DMA controller, a round-robin priority algorithm is used to arbitrate between the competing requests.)

The transfer of data in either direction typically uses a ring buffer defined within host memory. The ring buffer for transmit operations is defined by a closed linked list of Tx descriptors. The ring buffer for receive operations is defined by a closed linked list of Rx descriptors. The two ring buffers are formed of equal-sized segments, each of which is 32-bit aligned and is capable of storing a packet of up to the maximum size of packet transferred.

Once initialized, the DMA controller can be left unattended to continuously fill/empty the specified ring buffers. Software can use the DMA interrupts generated or poll semaphore bits within the descriptors to maintain synchronization with the packet streams.



Block Instantiation Diagram

The M-AHBE core uses a 32-bit AHB slave interface for control and observation of the DMA controller. This interface occupies 1 Kbyte of host address space.

Note: The M-AHBE bridge does not support cut-through type buffering operations at this time.

Tool Flow

The supplied testbenches have been run on different simulator software and different platforms before shipment in order to ensure correct operation at the licensee's facility. Among the tools used: Mentor Graphics ModelSim® and Cadence Verilog (native compile and cross compile). The code has been executed in both UNIX and PC environments.

Reference Technology Gate Count: approx. 5,000 gates

About Mentor Graphics Silicon-Proven, Standards-Based Intellectual Property

Mentor Graphics offers a variety of industry-leading, standards-based IP cores that are rigorously tested and validated to provide design teams with the most reliable cores in the industry. Mentor's IP portfolio ranges from simple SoC building blocks, such as communications interfaces and microcontrollers, to an expansive offering of products for Ethernet, USB, Storage, and PCI Express.

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