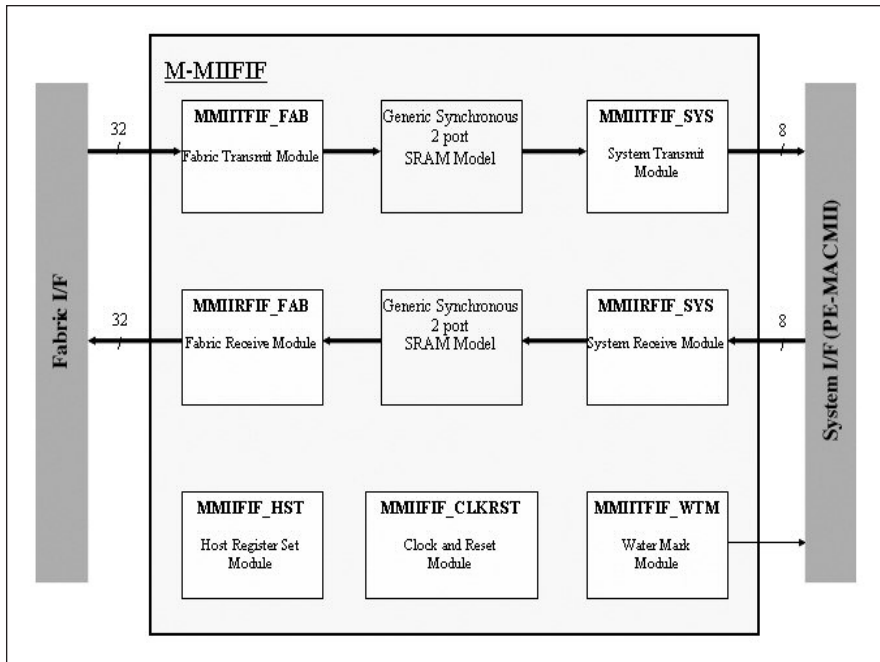


Ethernet IP

FIFO Memory Interface to the 10/100 Mbps Ethernet MAC

M-MIIFIF

D A T A S H E E T



M-MIIFIF sub-modules and data flow

Overview

The M-MIIFIF™ module from Mentor Graphics is a flexible FIFO module with transmit and receive buffering that can significantly improve the performance of embedded 10/100 Mbps Ethernet systems. It integrates with the PE-MACMII™ 10/100 Mbps Ethernet MAC module (also available from the Mentor Graphics Ethernet IP library) and functions in all of the PE-MACMII's modes.

The M-MIIFIF is a low gate count, easily synthesizable FIFO module that offers increased system level throughput via data queuing. Automatic pause frame handshaking and per transmit frame MAC configuration data are both supported.

Other features of this logic module are clock-frequency-independent I/O ports, single or multiple word I/O data transfers, and full memory utilization with graceful memory full frame drop. The M-MIIFIF module also provides programmable high and low receive storage level indicators and pause frame handshaking reassertion intervals, high transmit storage level indication, and CPU frame insertion and inspection capabilities.

The M-MIIFIF module is provided in Verilog RTL source code, with a full test suite and module level documentation.

The M-MIIFIF uses synchronous dual-port memories.

Major product features:

- Operates at 10- or 100-Mbps
- Provides data queuing for increased system level throughput
- User definable storage sizes
- Clock frequency independent I/O ports
- Single or multiple word data transfers
- Programmable Rx and Tx storage level indicators, plus Tx storage under-run indication
- CPU frame insertion and inspection
- Automatic pause frame handshaking
- Programmable pause frame handshaking reassertion interval
- Graceful Rx memory full frame drop
- Graceful enable and disable
- Programmable frame or word cut-through threshold
- Tx storage frame rewind capabilities
- Full memory utilization
- Optional per transmit frame MAC configuration data supported
- Low gate count
- Fully synthesizable
- Scan, insertion-friendly design
- Uses synchronous dual-port memories

Deliverables:

- Verilog RTL source code
- Functional testbench
- Synopsys constraint files
- Module-level documentation

Structure

The M-MIIFIF consists of the following seven major RTL logic sub-modules:

- **MMIITFIF_FAB** – FIFO Fabric Transmit Interface Module
- **MMIITFIF_SYS** – FIFO System Transmit Interface Module
- **MMIIRFIF_FAB** – FIFO Fabric Receive Interface Module
- **MMIIRFIF_SYS** – FIFO System Receive Interface Module
- **MMIITFIF_WTM** – FIFO System Watermark Module
- **MMIIFIF_HST** – FIFO Host Interface Module
- **MMIIFIF_CLKRST** – FIFO Clock and Reset Module

Implementation

The M-MIIFIF module and the PE-MACMII core have been optimized for use in multiple-MAC applications. These include switches, multi-port-port interface cards, NICs, and routers. The exact nature of the common sections for system data transport, address recognition, and statistics will be application dependent, but the PE-MACMII and M-MIIFIF cores have enough built-in flexibility to cover almost any system concept.

Host Interface Options

The M-MIIFIF module and the PE-MACMII core connect to a host system. The host system may be of different types. In a switch system, the host will generally be the embedded CPU or the back plane switching fabric.

Testbenches

The M-MIIFIF is supplied with two testbenches, one verifies the M-MIIFIF when not integrated with the PE-MACMII, and the other verifies their operation together. Each testbench is described in a separate verification document.

Reference Technology Gate Count: approx. 15,000 gates plus RAM

About Mentor Graphics Silicon-Proven, Standards-Based Intellectual Property

Mentor Graphics offers a variety of industry-leading, standards-based IP cores that are rigorously tested and validated to provide design teams with the most reliable cores in the industry. Mentor's IP portfolio ranges from simple SoC building blocks, such as communications interfaces and microcontrollers, to an expansive offering of products for Ethernet, USB, Storage, and PCI Express.

Signal Descriptions

Clock and Reset Signals	
External hard reset; Reset bypass	Input
M-MIIFIF transmit clock (post tree)	Input
M-MIIFIF Fabric Tx clock (post tree)	Input
M-MIIFIF receive clock (post tree)	Input
M-MIIFIF Fabric Rx clock (post tree)	Output
Host I/F Signals	
Host reset	Input
Host clock	Input
Host chip select not	Input
Host read / write not	Input
Host address	Input
Host input data	Input
Host output data	Input
Host output data enable	Output
System Transmit I/F Signals	
M-MIIFIF transmit clock enable	Input
Transmit packet start of frame	Output
Transmit packet data	Output
Transmit packet end of frame	Output

Transmit packet under run	Output
Transmit packet control frame	Output
Transmit per packet override	Output
Transmit per packet pad mode; CRC mode	Output
Transmit packet need data	Input
Pause request	Output
Pause value	Output
Pause acknowledge	Input
Transmit packet retransmit	Input
Transmit packet abort	Input
System Receive I/F Signals	
M-MIIFIF receive Clock enable	Input
Receive packet start of frame	Input
System Receive data	Input
Receive packet data valid	Input
Receive packet end of frame	Input
Receive packet drop frame	Input
Receive statistics vector + pulse	Input
Receive unicast address match	Input

Fabric Transmit I/F Signals	
Fabric transmit ready	Input
Fabric transmit accept	Output
Fabric transmit start of frame; end of frame	Input
Fabric transmit frame data	Input
Fabric transmit data not valid	Input
Fabric transmit per packet enable	Input
Fabric transmit per packet generate FCS	Input
Fabric transmit per packet pad mode	Input
Fabric transmit control frame	Input
Fabric transmit high watermark	Input
Fabric Receive I/F Signals	
Fabric receive accept	Input
Fabric receive start of frame; end of frame	Output
Fabric receive frame data	Output
Fabric receive data not valid	Output

Visit www.mentor.com/ip for more information on our complete IP portfolio of Storage, Ethernet, USB, and PCI Express products.

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