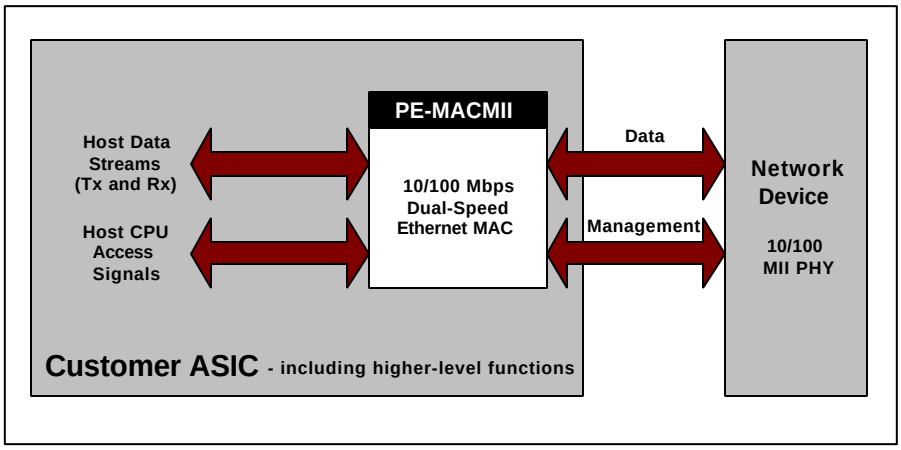
PE-MACMII™
10/100 Mbps Dual-Speed Ethernet MAC

Inventra™ Soft Core (RTL IP)

D A T A S H E E T



PE-MACMII Application

Overview

The PE-MACMII™ provides a 10/100 Mbps Ethernet Media Access Controller (MAC) for incorporation in a customer's own ASIC design.

The PE-MACMII module consists of six sub-modules. These sub-modules comprise the transmit and receive portions of the Ethernet MAC plus three supporting sub-modules.

The core is adaptable to a wide range of system requirements. For example, it is designed to interface to 10 or 100 Mbps MII-based PHY devices but the range of PHYs supported can readily be extended by adding one of the optional interface modules that are available for the core. Similarly, the core offers a processor independent 16-bit host interface but can readily be interfaced to a range of standard buses through the addition of bridges such as the optional AMBA AHB Bridge provided with the PE-MACMII core (see 'Implementation', overleaf).

There are many different possible applications for the PE-MACMII, including network interface designs, Ethernet switching designs, and test equipment designs.

The PE-MACMII module was designed in Verilog. The core technology was originally shipped in 1995, and is currently shipping in silicon in millions of units per year.

The design may be synthesized in .5µm CMOS (or better). The nominal module size is approximately 11,000 gates.

Major Product Features:

- Supports 10 or 100 Mbps MII-based PHY devices including: 10Base-T, 100Base-TX, 100Base-FX, and 100Base-T4
- Supports IEEE 802.3x Full Duplex Flow Control and Half Duplex Back Pressure
- Meets ISO / IEC 802.3 and IEEE 802.3u specifications
- Meets VSIA's specification for a soft Virtual Component
- Optional interface modules available for RMII, SMII, ENDEC (10T) and PMD (100X)
- 16-bit host interface. Optional AMBA AHB bridge supplied with core.
- Additional PE-MSTAT register-based statistics module available
- Optimized for switching, multiport and embedded applications
- Fully synthesizable
- Scan insertion-friendly design

Deliverables:

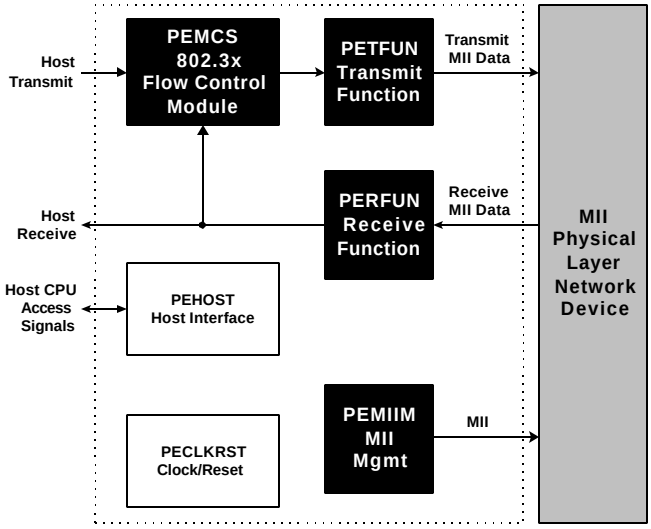
- Verilog source code
- Synthesis constraints files
- Functional testbench with documentation of the PE-MACMII's conformance to appropriate IEEE PICS
- Expanded Statistics vectors for certain RMON and Etherstats applications

Mentor Graphics is the leading supplier of a broad range of IP soft cores targeting standards-based communications applications. These highly re-usable cores help systems and chip designers get to market faster.

Structure

The PE-MACMII module consists of six sub-modules (as shown in the adjacent diagram). The six sub-modules can be thought of in two groups: MAC functions and supporting network I/O functions. The MAC functions are principally provided by the transmit and receive modules PETFUN and PERFUN. These modules must be included in every implementation. The 802.3x PAUSE frame function is implemented by the PEMCS module.

The Host interface needs to be tailored to the individual application. If the PE-MACMII module is used to create a multi-port device like a switch, the Host CPU interface will typically be to an embedded processor. In an end-station implementation, the interface might be to the end-station bus.



Layout of PE-MACMII module

Implementation

The PE-MACMII exports the transmit and receive packet streams directly to the top of the design, thereby allowing customer-specific DMA solutions to be readily connected to the core. This in turn allows the core's performance to be tailored to and optimized for each individual application.

The PE-MACMII module comes with a standard MII interface. However, due to market demands for additional interfaces, four optional PHY interfaces are offered as separate modules. These optional interfaces are:

- PE-SMII (Serial Media Independent Interface)
- PE-RMII (Reduced Media Independent Interface)
- PE-ENDEC (10T Interface), and
- PE-PMD (100X Interface).

The PE-MACMII also comes with a processor independent 16-bit host interface. However it can readily be interfaced to a range of standard buses through the addition of bridges such as the optional AMBA AHB Bridge provided by Inventra with the PE-MACMII core. This bridge features separate, double-buffered, TX and RX FIFOs of configurable size and a built-in DMA facility that is able to handle bursts of any size on the AHB.

The PE-MACMII AHB bridge transfers data across its host interface at 12.5MHz while the AHB can operate at any speed, higher, lower or identical to the PE-MACMII core speed. The necessary clock synchronization is carried out in the bridge.

Statistics Collection

The PE-MACMII transmit and receive functions are not instrumented with large numbers of counters for statistics collection. Instead, a vector-generation method is used.

Most activity in a MAC is centered on major events such as completion of packet reception or completion of packet transmission attempts. When these major events occur, the PE-MACMII module generates a statistics vector, summarizing the detailed results associated with the event. The vector is then latched into a statistics collection block. A vector is latched once for each major event.

This vector approach reduces the requirement for individual synchronization of many individual events. The approach also reduces the gate count by eliminating the need for flip-flops scattered around the MAC design.

The vector method is also more efficient in multiple-MAC systems. Statistics accumulation may be done centrally for all of the MACs in the system, reducing gate count and improving processing efficiency. A result of this approach is that the statistics gathering mechanism must be created on a case-by-case basis outside the MAC.

Reference Technology Gate Count: Core 11,000; Bridge 18,000 *(mainly contributed by the need to handle large data buses and synchronization between the different clock domains)*

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