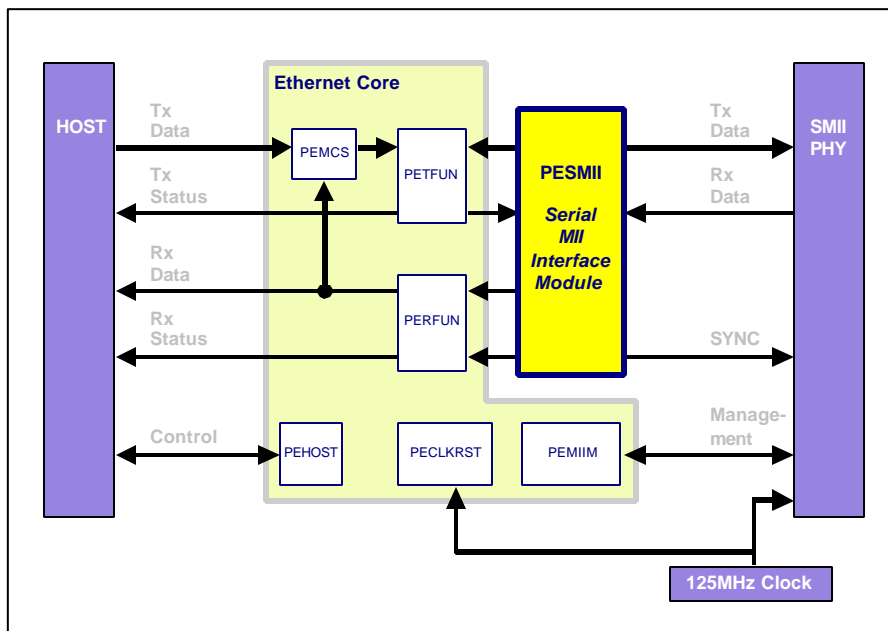


PE-SMII

Serial MII I/F for Inventra's Ethernet MACs

Inventra™ Soft Core (RTL IP)

D A T A S H E E T



PE-SMII Application

Overview

The PE-SMII pack provides a Serial MII Interface for a 10/100 Mbps Ethernet MAC to be used with PHYs that offer two pins per port. The Ethernet MAC core is also available in the Mentor Graphics Inventra™ range of soft cores.

The required 2-signal + clock and synchronization interface to the PHY is provided by the PESMII module within the PE-SMII pack. This module performs the conversion of the 4-bit MII data handled by the basic MAC design to/from the serial data format of the Serial-MII interface in both the transmit and the receive directions. The registers within the PHY are read and written through the MAC's Host Interface.

The combination of the Ethernet MAC core with the PE-SMII interface is intended for incorporation in a customer's own ASIC design. Both 10 Mbps and 100 Mbps operational speeds are supported.

There are many different possible applications, including Network Interface designs, Ethernet Switching designs and test equipment designs.

The PESMII module was designed in Verilog and may be synthesized in .5µm CMOS (or better). The module synthesizes to approximately 1,600 gates.

Major Product Features:

- Works with Inventra's 10/100Mbps Ethernet MACs
- Provides interface to 2-pin-per-port PHYs
- Adheres to Serial-MII Specification v1.2
- Optimized for switching, multiport and embedded applications
- Fully synthesizable
- Scan insertion-friendly design

Deliverables:

- Verilog source of PESMII module
- Wrapper integrating PESMII module with MAC core modules
- Synthesis constraints files
- Functional testbench
- Design documentation

Related Products:

- PE-MCXMAC 10/100/1000 Ethernet MAC
- PE-MACMII™ 10/100 Ethernet MAC
- PE-RMII RMII interface for PE-MACMII
- PE-PMD TP-PMD (100X) interface for PE-MACMII
- PE-ENDEC 10T interface for PE-MACMII
- PE-MSTAT™ Statistics Package
- PE-SAL™ Station Address Logic Module

Mentor Graphics is the leading supplier of a broad range of IP soft cores targeting standards-based communications applications. These highly re-usable cores help systems and chip designers get to market faster.

PE-SMII: Serial MII I/F for Inventra's Ethernet MAC Soft Cores

Functional Overview

The PE-SMII pack provides a Serial Media Independent Interface for Inventra's 10/100 Mbps Ethernet MAC soft cores.

The interface between the 16-signal MII interface and the two-signal Serial-MII interface is provided by the PESMII module within the PE-SMII pack.

In the transmit direction, MAC core generates MII nibble data streams in response to frame byte streams supplied by the host system. The PESMII takes the nibble data, which is clocked at 25 MHz (2.5 MHz in 10 Mbps mode), and outputs serial data at the SMII Reference Clock frequency of 125 MHz. A synchronizing pulse is asserted every 10th clock to signal the start of a new 10-bit segment comprising a Transmit Enable bit, a Transmit Error bit followed by a byte of data.

In 100 Mbps mode, each segment conveys one byte of data. In 10 Mbps mode, each segment is repeated ten times, thus modulating the bandwidth down to 10 Mbps.

In the receive direction, the SMII PHY provides serial data synchronous to the reference clock. Again 10-bit segments are transferred with the start marked by a SYNC pulse. The first two bits represent Carrier Sense and Receive Data Valid. The remaining eight bits represent one byte of data. In 100 Mbps mode, a new nibble is output each RX_CLK. In 10 Mbps mode, the SMII PHY replicates each received byte ten times and the PESMII only needs to pass a nibble to the MAC every tenth RX_CLK.

During inter-packet-gaps, the SMII PHY conveys link status information. The PESMII monitors the link status and reflects this via the host interface status signals. The PESMII also samples the first status segment following a packet to check for RX_ER and Dribble Nibble. The packet being passed to the MAC is pipelined in order to allow proper signaling of these conditions. The PESMII also monitors the status segment for False Carrier indications and conveys to the MAC any that occur.

As soon as non-idles are detected on the medium, this is conveyed to the MAC via the Carrier Sense bit in the receive segment. With both ends of the link using a locally supplied reference clock, an elasticity FIFO is required within the PHY because the passage of the receive data through this FIFO needs to be de-coupled from the Carrier Sense indication.

The PESMII also allows MAC to MAC connections. In such applications, both MACs should be configured for 100 Mbps, Full-Duplex (MAC-MAC) operation. Should other PESMII signal status vary from these pre-configured values, a CLASH will be signaled to the host module for software intervention. Packet integrity cannot be assured in such circumstances.

Using the PE-SMII pack

The PE-SMII pack is solely for use with Inventra's Ethernet MAC cores and so will typically be purchased alongside the MAC core.

Purchasing the PE-SMII pack not only gives you the PESMII module but also a top-level wrapper in which the PESMII module is instantiated alongside the modules of the Ethernet MAC cores.

Implementation

The combined system of the Ethernet MAC with the PE-SMII interface exports the transmit and receive packet streams directly to the top of the design, thereby allowing customer-specific DMA solutions to be readily connected to the core. This in turn allows the MAC's performance to be tailored to and optimized for each individual application.

The Host interface needs to be tailored to the individual application. Where the MAC is used in a multi-port device like a switch, the Host CPU interface will typically be to an embedded processor. In an end-station implementation, the interface might be to the end-station bus.

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