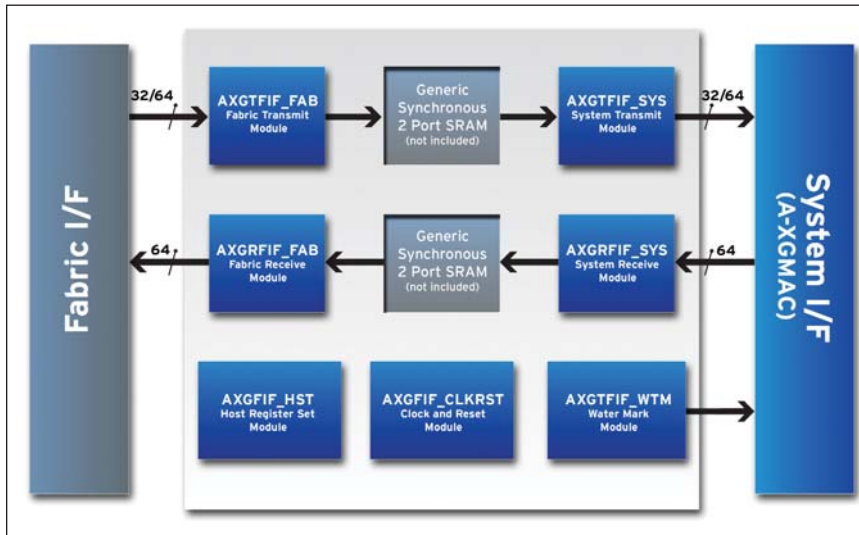


Ethernet IP

10-Gigabit Ethernet FIFO Memory Interface

A-XGFIF

D A T A S H E E T



A-XGFIF submodules and data flow.

10-Gig Ethernet FIFO Available in Two Versions

Mentor Graphics® A-XGFIF is a low gate count, easy-to-synthesize 10-Gbps FIFO module that offers increased system-level throughput by allowing data queuing. The A-XGFIF module seamlessly integrates with Mentor's A-XGMAC 10-Gbps Ethernet MAC module.

The A-XGFIF is a feature-rich FIFO module including automatic pause-frame handshaking and support for per-frame-MAC-configuration overrides. Other features of the A-XGFIF core include clock frequency independent I/O ports, single or multiple word I/O data transfers, full memory utilization with graceful Receive memory-overflow recovery. The A-XGFIF module also provides programmable high and low Receive memory level indicators and pause-frame handshaking reassertion intervals, high Transmit memory level indication, and CPU frame insertion and inspection capabilities.

The A-XGFIF IP core consists of two different versions of the FIFO. The smaller asymmetric (32-bit Transmit and 64-bit Receive data) data path version which has been optimized for ASIC implementations and the larger, symmetric (64-bit Transmit and Receive data) data path version which can be implemented in FPGA-based devices. The basic structure of the A-XGFIF core is the same and consists of seven major submodules as depicted in the above diagram.

Mentor's A-XGFIF and A-XGMAC modules can be used in many different applications, but their speed makes them best suited for switches, multi-port bridges, and routers. The A-XGFIF is ideal for use with synchronous dual-port memories.

Major product features:

- User-definable memory sizes
- Signal or multiple word transfers
- Programmable high and low receive memory level indicators
- Automatic pause frame handshaking
- Programmable high-transmit memory level indicator
- Graceful Rx memory overflow handling
- Tx memory under run indication
- Tx memory frame rewind capability
- Full utilization of synchronous dual-port memories
- Optional per transmit frame MAC configuration support

Deliverables:

- Verilog RTL source code
- Functional testbench
- Synthesis constraints files
- Module-level documentation

Related products:

- **A-XGMAC** - 10-Gigabit Ethernet MAC core
- **A-XGL2P** - 10-Gigabit Layer 2 subsystem for FPGA devices
- **M-XGXS** - XGMII to XAUI conversion module
- **M-XGPCSR** - 10-Gigabit PCS layer for 10GBASE-R applications

Functional Description

The A-XGFIF core consists of seven major submodules:

The **AXGTFIF_FAB** submodule handles the transferring of data from the Fabric bus or external DMA controller with support for either single word transfers or large bursts of data. The AXGTFIF_FAB module uses a generic request/acknowledge handshake scheme to control the flow of data into the memory modules.

Signal Descriptions:

Host Interface Signals		
Signal	Type	Description
MSTRST	Input	Master Reset
HSTRST	Input	Host Reset
HSTCLK	Input	Host Clock
HSTCSN	Input	Host Chip Select not
HSTWRN	Input	Host read / write port
HSTADX[7:0]	Input	Host Register Address
HSTIDAT[31:0]	Input	Host Input Data
HSTODAT[31:0]	Output	Host Output Data
HSTOE	Output	Host Output Data Enable
System Transmit Interface Signals		
MTCLK	Input	Transmit Clock (312.5MHZ or 156.25MHz)
STSOF	Output	System Transmit Start of Frame Indicator
STSTRM	Input	System Transmit Stream Data Indicator
STDAT[x:0]	Output	System Transmit Data x = 31 or 63 based on Transmit module selection
STDATNVLD[y:0]	Output	System Transmit Data Valid (Bytes) y = 1 or 2 based on Transmit module selection
STEOF	Output	System Transmit End of Frame Indicator
STABRT	Output	System Transmit Abort Indicator
STCFRM	Output	System Transmit Control Frame Indicator
STPPEN	Output	System Transmit Per Packet Override Qualifier
STPPADMODE[1:0]	Output	System Transmit Per Packet Pad Mode
STPPGENFCS	Output	System Transmit Per Packet FCS Append
STPPDLFCS[1:0]	Output	System Transmit Per Packet Delay FCS
PSREQ	Output	System Pause Request
PSVAL	Output	System Pause Frame Value (Xon/Xoff)
PSACK	Input	System Pause Request Acknowledge
System Receive Interface Signals		
MRCLK	Input	Receive Clock (156.25MHz)
RSOF	Input	System Receive Start of Frame Indicator
SRDAT[63:0]	Input	System Receive Data
SRDATNVLD[2:0]	Input	System Receive Data Valid (Bytes)
SREOF	Input	System Receive End of Frame Indicator
SRDRPFM	Input	System Receive Drop Frame Indicator
Fabric Transmit Interface Signals		
FTCLK	Input	Fabric Transmit Clock
FTRDY	Input	Fabric Transmit Ready
FTACPT	Output	Fabric Transmit Accept
FTSOF	Input	Fabric Transmit Start of Frame Indicator
FTEOF	Input	Fabric Transmit End of Frame Indicator
FTDAT[x:0]	Input	Fabric Transmit Data x = 31 or 63 based on Transmit module selection
FTDATNVLD[y:0]	Input	Fabric Transmit Data Valid (Bytes) y = 1 or 2 based on Transmit module selection
FTPPEN	Input	Fabric Transmit Per Packet Override Qualifier
FTPPGENFCS	Input	Fabric Transmit Per Packet FCS Append
FTPPADMODE[1:0]	Input	Fabric Transmit Per Packet Pad Mode
FTCFRM	Input	Fabric Transmit Control Frame Indicator
FTHWM	Output	Fabric Transmit High Watermark Indicator
Fabric Receive Interface Signals		
FRCLK	Input	Fabric Receive Clock
FRRDY	Output	Fabric Receive Ready
FRACPT	Input	Fabric Receive Accept
FRSOF	Output	Fabric Receive Start of Frame Indicator
FREOF	Output	Fabric Receive End of Frame Indicator
FRDAT[63:0]	Output	Fabric Receive Data
FRDATNVLD[2:0]	Output	Fabric Receive Data Valid (Bytes)

The **AXGTFIF_SYS** submodule reads the data out of the memory and interfaces with the A-XGMAC core's system interface through the use of a streaming word interface. The AXGTFIF_SYS module also handles the Flow control interface signals which transmits the pause frames onto the link.

The **AXGRFIF_FAB** and **AXGRFIF_SYS** submodules accept the incoming Receive data from the A-XGMAC core, implement any requested frame filtering conditions, and output the valid Receive data to the system's Fabric interface or external DMA controller. The AXGRFIF_FAB submodule uses a generic request/acknowledge handshake scheme to control the flow of data out of the memory modules.

The **AXGTFIF_WTM** submodule is responsible for handshaking the Transmit and Receive read/write pointers between the Fabric and MAC side clock domains. The AXGTFIF_WTM module also contains all of the watermarking logic and updates the appropriate watermark signals in the A-XGFIF core.

The **AXGFIF_HST** module contains all of the A-XGFIF's configuration and status registers. The **AXGFIF_CLKRST** module handles any clock division and the necessary synchronization logic for resets signals.

The A-XGFIF core includes two different versions of the AXGTFIF_FAB and AXGTFIF_SYS modules for support of the asymmetric (32-bit) and symmetric (64-bit) Transmit data paths. The asymmetric data path allows ASIC designers to take advantage of today's smaller geometries by running the MAC side Transmit logic at 312.5MHz instead of the more common 156.25MHz, realizing 50 percent savings in area. The symmetric data path is available for designers looking at FPGA devices for prototyping or as an end product.

Reference Technology Gate Count:

- Asymmetric: 12,000 + RAM
- Symmetric: 20,000 + RAM

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