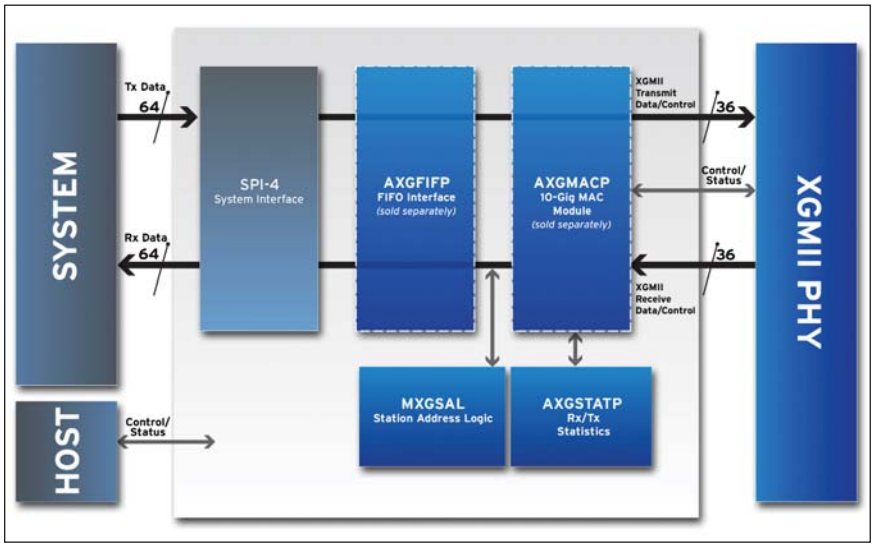
A-XGL2P

D A T A S H E E T

Ethernet IP

10-Gigabit Ethernet Layer 2



A-XGL2P submodules and data flow.

Ideal for Programmable Logic (FPGA) Implementations

Mentor Graphics® A-XGL2P IP core provides a complete IEEE 802.3ae Ethernet Layer 2 solution when incorporating Mentor's A-XGMAC and A-XGFIF IP products. The completely integrated solution comprises a Logical Link Control, MAC Control, MAC, and reconciliation sublayer for a 10-Gbps interface between the Network Layer (Layer 3) and Physical Layer (Layer 1) of the Ethernet OSI model. The A-XGL2P offers an IEEE 802.3ae XGMII interface for the link, and an SPI-4 phase 1 compatible interconnect for the fabric interface. There is also a Host interface for register access.

All of the modules in the A-XGL2P IP core have been written specifically to allow implementation in slower technologies, thus allowing easy verification of designs that involve the A-XGL2P in FPGA technologies.

Major product features:

- Compliance with IEEE 802.3ae
- Support for IEEE 802.3x Full Duplex Flow control
- Support for 802.3ae XGMII
- Programmable Drop/Receive frame filter
- 33 statistics counters supporting RMON and EtherStats applications
- IPG dithering for XGMII alignment and average min. IPG maintenance
- XGMII local and remote link fault detection
- Programmable MAC station address
- MII Management (MDIO) support: preamble suppression, hardware polling, MDC frequency selection, and indirect addressing
- SPI-4 compatible interface supporting full AXGMACP pipe and 10-Gbps data rate
- 8K/4K FIFO Receive/transmit buffer

Deliverables:

- Verilog RTL source code
- FPGA-specific constraint and project files
- Verilog functional testbench and associated documentation
- Design documentation

Related products:

- **A-XGMAC** - 10-Gigabit Ethernet MAC core
- **A-XGFIF** - 10-Gigabit FIFO core

Functional Description:

The A-XGL2P consists of five major blocks: AXGMACP (part of A-XGMAC deliverables); AXGFIFP (part of A-XGFIF deliverables); SPI-4; AXGSTATP; and MXGSAL. (All are depicted in the diagram on the front page.)

The **AXGMACP** 10-Gbps Ethernet MAC module performs packet transmission and reception protocol as described in IEEE 802.3ae. It also includes the MAC control sublayer, as defined in 802.3x.

The **AXGFIFP** 10-Gbps FIFO Interface module provides a data buffering FIFO for communication between the AXGMACP Ethernet interface and the SPI-4 compatible system interface.

Signal Descriptions:

Signal	Type	Description
Host Interface Signals		
MSTRRST	Input	Master Reset
HSTRST	Input	Host Reset
HSTCLK	Input	Host Clock
HSTCSN	Input	Host Chip Select not
HSTWRN	Input	Host read / write port
HSTADX[7:0]	Input	Host Register Address
HSTIDAT[31:0]	Input	Host Input Data
HSTODAT[31:0]	Output	Host Output Data
HSTOE	Output	Host Output Data Enable
HSTACK	Output	Host Acknowledge
HSTINT	Output	Host Interrupt
SPI4 Transmit Interface Signals		
FTCLK	Input	Fabric Transmit Data Clock , 200Mhz Maximum
TXADDR[3:0]	Input	Transmit Address
TXDATA[63:0]	Input	Transmit Data
TXEOP	Input	Transmit End of Cell or Packet Indicator
TXERROR	Input	Transmit Data Error
TXPRTY[3:0]	Input	Transmit Data Parity Indicator
TXSIZE[2:0]	Input	Transmit Data Size Indicator
TXSOCP	Input	Transmit Start of Cell or Packet Indicator
TXVALID	Input	Transmit Data Valid
TXFULL[3:0]	Output	Transmit Buffer Full Indicators
TXSTART	Output	Transmit Start Indicator
MTCLKI	Input	MAC Transmit Clock, 156.25MHz
SPI4 Receive Interface Signals		
RXCLK	Output	SPI4 Receive Clock
FRCLKI	Input	Fabric Receive Data Clock, 200MHz Maximum
RXADDR[3:0]	Output	Receive Address
RXDATA[63:0]	Output	Receive Data
RXEOP	Output	Receive End of Cell or Packet Indicator
RXERROR	Output	Receive Data Error
RXPRTY[3:0]	Output	Receive Data Parity Indicator
RXSIZE[2:0]	Output	Receive Data Size Indicator
RXSOCP	Output	Receive Start of Cell or Packet Indicator
RXVALID	Output	Receive Data Valid
RXFULL[3:0]	Input	Receive Buffer Full Indicators
RXSTART	Input	Receive Start Fill Indicator
XGMII Data Interface Signals		
XGTMIICLK	Output	XGMII Transmit Clock (156.25MHz, SDR or DDR)
XGTMII[71/35:0]	Output	XGMII Transmit Data and Control Signals
XGRMIICLK	Input	XGMII Receive Clock (156.25MHz, SDR or DDR)
XGRMII[71/35:0]	Input	XGMII Receive Data and Control Signals
MII Management Interface Signals		
MDIO	Input	MIIM Serial Data In/Out
MDC	Output	MIIM Clock

The **SPI-4** (System Physical Interface Level 4) module provides a system-compatible interface for connecting between the Physical Layer (Layer 1) and Link Layer (Layer 3), or between peer-to-peer entities operating at OC-192 rate.

The **AXGSTATP** 10-Gbps Statistics module is a low gate count, register-based statistics module developed for integration with the AXGMACP.

The **MXGSAL** 10-Gbps Station Address Logic module takes the destination address field of incoming packets and all related control signals and performs a hashed address comparison for help in address-based frame filtering.

Functionality

The main 802.3ae functionality is provided by the AXGMACP 10-Gbps Ethernet MAC submodule, which is included with the A-XGMAC deliverables. The A-XGL2P has three main interfaces: SPI-4, Host, and XGMII. The SPI-4 compatible interface allows access to the data transmitted and received by the A-XGL2P. The Host interface allows access to the configuration registers of the submodules. The third interface allows access to XGMII-formatted PHY data.

The high-speed data is buffered between the SPI-4 compatible interface and the AXGMACP by separate Transmit (4K) and Receive (8K) FIFOs, which are defined in the AXGFIFP submodule. The A-XGL2P also includes statistics gathering and station address functions. Statistics information is gathered from the data transmitted and received over the Ethernet link by the AXGSTATP submodule, while the MXGSAL submodule provides address filtering and multicast reception capability. The register and data information of both submodules is accessed using the host interface.

Reference Technology Gate Count:

Altera Stratix II Devices

- Total ALUTs: 7657
- Total Registers: 6182
- Total PLLs: 2
- Total Memory Bits: 108,544

ASIC Gate Count

- Approx. 120,000 gates

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Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

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