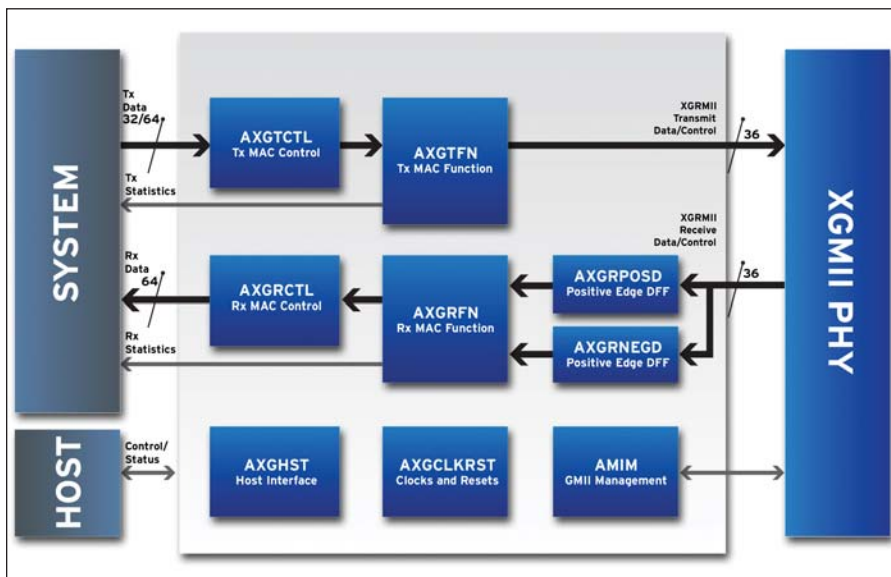


Ethernet IP

10-Gigabit Ethernet MAC

A-XGMAC

D A T A S H E E T



A-XGMAC submodules and data flow.

An IP Solution for 10-Gig Ethernet Products

The Mentor Graphics® A-XGMAC provides a 10-Gbps Ethernet Media Access Controller (MAC) for incorporation in a customer's own ASIC or FPGA-based design. The A-XGMAC module performs the packet transmission and reception protocol as described in IEEE 802.3ae. This includes having a MAC control sublayer as defined in 802.3x. The optional SONET OC-192 data rate control in Clause 46 is also implemented.

The A-XGMAC IP core consists of two different versions of the 10-Gig MAC. The smaller asymmetric (32-bit Transmit data and 64-bit Receive data) data path version which has been optimized for ASIC implementations and the larger symmetric (64-bit Transmit and Receive data paths) data path version which can be implemented in FPGA-based devices. The basic structure of the A-XGMAC core is the same and consists of seven major submodules as shown in the diagram above.

There are many possible applications for the A-XGMAC including network interface designs, Ethernet switching designs, and test equipment designs.

Major product features:

- Supports IEEE 802.3ae and IEEE 802.3x Full Duplex Control
- Programmable Drop Rx Frame Filter
- Per frame and default programmable padding and FSC insertion
- Support for externally generated proprietary control frames
- Synchronous or asynchronous configuration register access
- Separate MAC control sublayer hierarchy for ease and removal
- Packet-aware real time submodule enabling and disabling
- Frame reception relaxation, programmable for non-compliant PHYs

Deliverables:

- Verilog RTL source code
- Synthesis constraints files
- Verilog functional testbench with documentation of the A-XGMAC's conformance to appropriate IEEE PICS
- Detailed specifications including submodules, verification plan, and release history

Related products:

- **A-XGFIF** - Configurable FIFO module
- **M-XGXS** - XGMII to XAUI conversion module
- **M-XGPCSR** - 10-Gigabit PCS layer for 10G BASE-R applications
- **A-XGL2P** - 10-Gigabit Layer 2 subsystem for FPGA devices

Functional Description:

The A-XGMAC core consists of five submodules as depicted in the diagram on the front page.

The **AXGTFN** module performs all of the transmit specific functions defined by the IEEE specification for XGMII Transmit data including generation of preamble/SFD, IPG dithering, FCS generation, and proper lane alignment of the transmit data.

Signal Descriptions:

Host Interface Signals		
Signal	Type	Description
MSTRRST	Input	Master Reset
HSTRST	Input	Host Reset
HSTCLK	Input	Host Clock
HSTCSN	Input	Host Chip Select not
HSTWRN	Input	Host read / write port
HSTADX[7:0]	Input	Host Register Address
HSTIDAT[31:0]	Input	Host Input Data
HSTODAT[31:0]	Output	Host Output Data
HSTOE	Output	Host Output Data Enable
System Transmit Interface Signals		
MTCLK	Input	Transmit Clock (312.5MHz z or 156.25MHz)
STSOD	Input	System Transmit Start of Frame Indicator
STSTRM	Output	System Transmit Stream Data Indicator
STDAT[x:0]	Input	System Transmit Data
STDATNVLD[y:0]	Input	x = 31 or 63 based on Transmit module selection System Transmit Data Valid (Bytes) y = 1 or 2 based on Transmit module selection
STEOD	Input	System Transmit End of Frame Indicator
STABRT	Input	System Transmit Abort Indicator
STPPEN	Input	System Transmit Per Packet Override Qualifier
STPPADMODE[1:0]	Input	System Transmit Per Packet Pad Mode
STPPGENFCS	Input	System Transmit Per Packet FCS Append
STPPDLYFCS[1:0]	Input	System Transmit Per Packet Delay FCS
SRPAUSREQ	Input	System Receive Pause Request
SRPAUSVAL[15:0]	Input	System Receive Pause Frame Value
SRPAUSACK	Output	System Receive Pause Request Acknowledge
TSVP	Output	Transmit Statistics Indicator
TSV[51:0]	Output	Transmit Statistics Vector
System Receive Interface Signals		
MRCLK	Input	Receive Clock (156.25MHz)
SRSOD	Output	System Receive Start of Frame Indicator
SRDAT[63:0]	Output	System Receive Data
SRDATNVLD[2:0]	Output	System Receive Data Valid (Bytes)
SREOD	Output	System Receive End of Frame Indicator
SRDRPRFM	Output	System Receive Drop Frame Indicator
RSVP	Output	Receive Statistics Indicator
RSV[31:0]	Output	Receive Statistics Vector
XGMII Data Interface Signals		
XGMTIICLK	Output	XGMII Transmit Clock (156.25MHz, DDR)
XGMTII[35:0]	Output	XGMII Transmit Data and Control Signals
XGRMIICLK	Input	XGMII Receive Clock (156.25MHz, DDR)
XGRMII[35:0]	Input	XGMII Receive Data and Control Signals
MIIM Management Interface Signals		
MDI	Input	MIIM Serial Data In
MDC	Output	MIIM Clock
MDO	Output	MIIM Serial Data Out
MDOF	Output	MIIM Output Data Enable

The **AXGRFN** module includes the IEEE defined receive functionality for XGMII Receive data and checks for valid IEEE Ethernet frames. It also handles the transfer of the DDR-based XGMII Receive data to a 64-bit data bus.

The **AXGRCTL** and **AXGTCTL** modules implement the 802.3x Flow control functionality for support of Pause control frames. The **AXGTCTL** module generates proper Pause frames as requested by the system interface and enforces the halting of data transmission when valid Pause frames are received and verified by the **AXGRCTL** module.

The **AXGHST** module contains all of the A-XGMAC's configuration and status registers. It also interfaces with the **AMIIM** module of implementation of the MII Management interface for communicating with up to 31 different PHY devices through the MDIO interface. The **AXGCLKRST** module handles any clock divisions or synchronization logic for resets signals.

The A-XGMAC core includes two different versions of the **AXGTFN** and **AXGTCTL** modules for support of the asymmetric (32-bit) and symmetric (64-bit) Transmit data paths. The asymmetric data path allows ASIC designers to take advantage of today's smaller geometries by running the Transmit logic at 312.5MHz (instead of the more common 156.25MHz) while realizing 50 percent savings in area versus the 156.25MHz clock data bus. The symmetric data path is available for designers looking at FPGA devices for prototyping or as an end product.

Reference Technology Gate Count:

- Asymmetric 44,000
- Symmetric 98,000

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MGC - 08/07 1026030-w