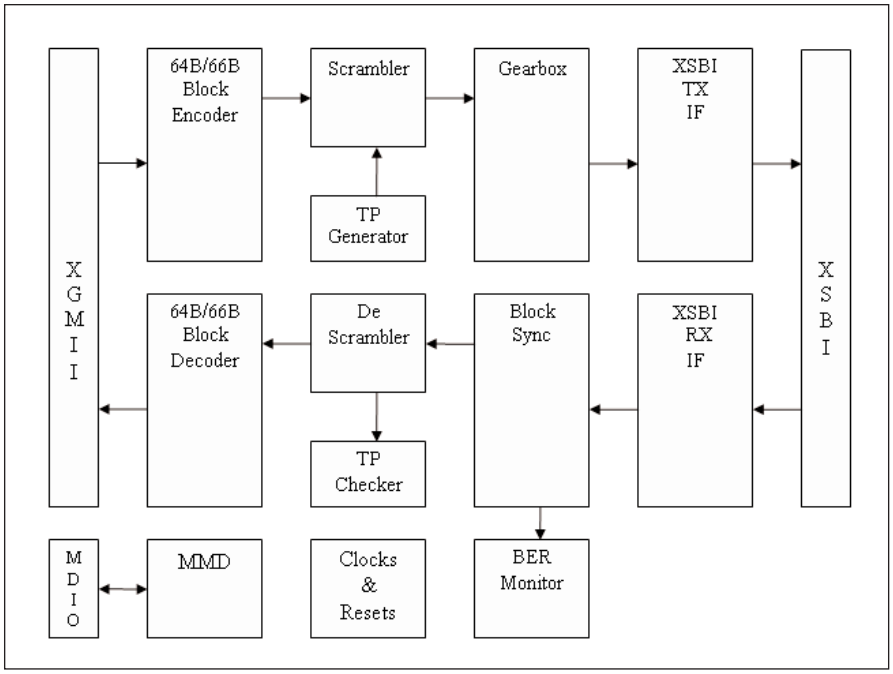
Ethernet IP

10 Gigabit BASE-R Physical Coding Sublayer

M-XGPCSR

D A T A S H E E T



M-XGPCSR sub-modules and data flow

Overview

The M-XGPCSR™ module from the Mentor Graphics Corporation implements the IEEE 803ae Clause 49 10-Gigabit PCS-R function. This function is located between the reconciliation sublayer (RS) and the PMA sublayer.

The M-XGPCSR connects to the RS side (MAC) with a 36-bit DDR interface or a 72-bit SDR interface for both Tx and Rx. On the PMA side, it connects with either the 16-bit (XSBI) interface or a 64-bit SDR interface for both Tx and Rx. The M-XGPCSR also implements Clause 45 to provide control and status through the management data input/output (MDIO) interface.

The M-XGPCSR is written in Verilog RTL and comes with a stand alone verification environment. In addition, synthesis scripts are supplied for TSMC 0.13um ASIC library and Altera StratixII FPGA. These scripts can easily be adapted to other technologies.

Major product features:

- Implements IEEE 802.3ae Clause 49
  - 10-Gigabit full duplex PCS
- XGMII interface to MAC devices
  - 32-bit DDR data interface
  - 4-bit DDR control interface
  - 156.25MHz clock
- XSBI interface to PMA SerDes devices
  - 16-bit source synchronous interface at 644.53MHz
- Rate adaptation between the XGMII clocks and XSBI clocks
- 64B/66B block encoding/decoding
- Scrambling/de-scrambling
- PRBS31 test pattern generation/checking
- BER checking
- Supports loopback
- Supports MDIO interface
- Supports Altera Stratix II FPGA devices

Deliverables:

- Verilog source code
- Detailed design documentation
- Synthesis constraints files
- Functional testbench with documentation
- Wrapper integrating the M-XGPCSR with Mentor's A-XGMAC core

Related products:

- A-XGMAC™ 10Gbps Ethernet MAC core
- A-XGFIF™ 10Gbps FIFO module
- M-XGXS™ XAUI XGMII extender

Mentor Graphics®

Functional Overview

In the transmit channel the 64B/66B block encoder maps XGMII data and control into 64B/66B blocks. The scrambler then scrambles the 64-bit data portion using the polynomial $G(x) = 1 + x^{39} + x^{58}$. The gearbox merges two sync bits with the scrambled data and rate adapts 10 Gb/s to 10.3125 Gb/s. The XSBI TX IF block implements a 4:1 mux using one SerDes per channel to achieve 16 channels of 644.53 Mb/s.

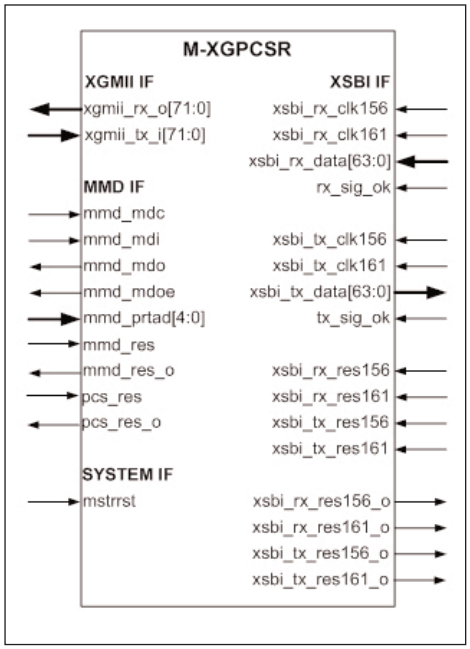
In the receive channel the XSBI RX IF block converts 16 channels of 644.53 Mb/s into 64 bits of raw data. The block sync uses the sync bits to find the block boundary of the 64B/66B blocks. The 64 bits of scrambled data is then sent to the de-scrambler. The 64B/66B block decoder converts the 64B/66B block back into XGMII data and control. The BER monitor ensures that the bit errors are below a threshold and sets a flag if it is exceeded.

The MMD block implements Clause 45 and contains all the registers associated with the PCS function.

The TP generator block generates pseudo random test patterns with the scrambler. The user can change the test pattern characteristics via the MMD block. The TP checker block validates the pseudo random test patterns.

The PRBS31 generator creates patterns according to the polynomial $G(x) = 1+x^{28}+x^{31}$. The PRBS31 checker validates the PRBS31 patterns.

The resets block generates synchronous resets for the different clock domains.



Block Instantiation Diagram

Standards Support

The M-XGPCSR supports both the IEEE 802.3ae (Draft 5.0) Clause 49 standard and the 802.3 Clause 45 standard.

Tool Flow

The supplied testbenches have been run on different simulator software and different platforms before shipment in order to ensure correct operation at the licensee's facility. Among the tools used: Cadence Verilog NC (native compile), Cadence Verilog (cross compile), and Mentor Graphics ModelSim®. The code has been executed in both UNIX and PC environments.

In addition, the Verilog RTL has been constrained and synthesized by Synopsys Design Compiler using third party standard cell libraries. The libraries were selected to be representative of the current technology at the time of testing. The constraints and design rules used during this process are intended to be generic in nature.

Reference Technology Gate Count: approx. 48,000 gates

About Mentor Graphics Silicon-Proven, Standards-Based Intellectual Property

Mentor Graphics offers a variety of industry-leading, standards-based IP cores that are rigorously tested and validated to provide design teams with the most reliable cores in the industry. Mentor's IP portfolio ranges from simple SoC building blocks, such as communications interfaces and microcontrollers, to an expansive offering of products for Ethernet, USB, Storage, and PCI Express.

Visit www.mentor.com/ip for more information on our complete IP portfolio of Storage, Ethernet, USB, and PCI Express products.

Copyright © 2005 Mentor Graphics Corporation.
M-XGPCSR, A-XGMAC, A-XGFIF, and M-XGXS are trademarks and Mentor Graphics and ModelSim are registered trademarks of Mentor Graphics Corporation.
All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

4-05 C&A 1023500-w