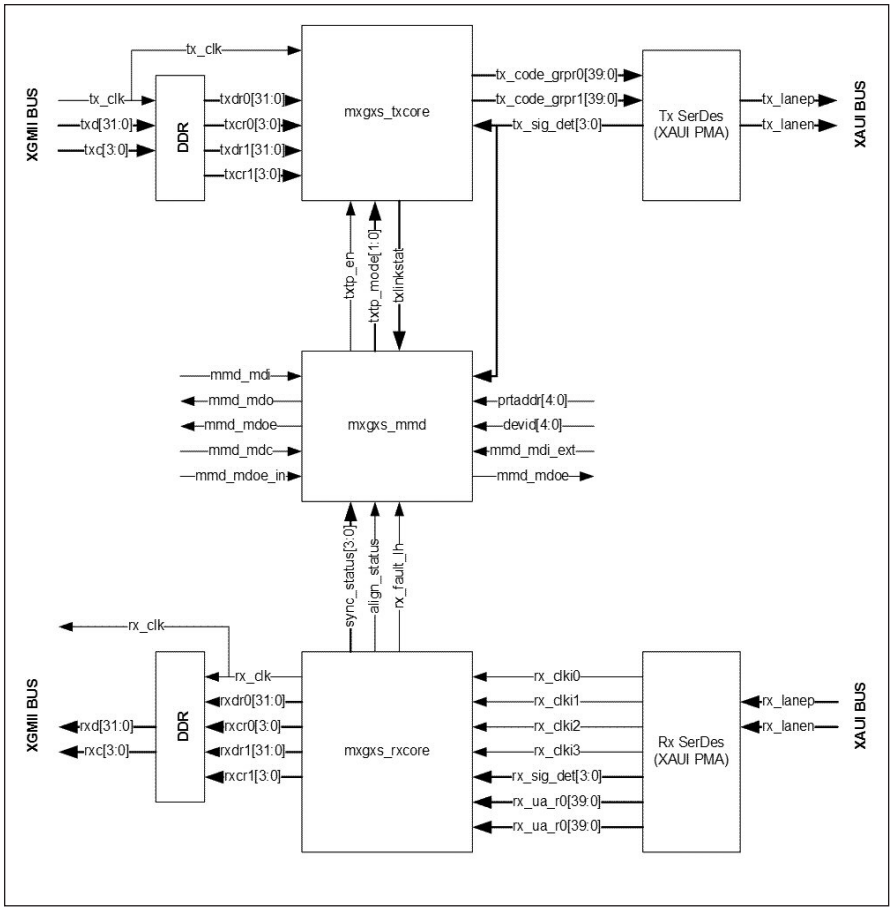
Ethernet IP

XAUI XGMII Extender

M-XGXS

D A T A S H E E T



M-XGXS sub-modules and data flow

Ethernet IP XAUI XGMII Extender

The M-XGXS™ module from Mentor Graphics provides the physical coding sublayer (PCS) functionality for transfer of Ethernet-based data between a 10-Gbps Ethernet media access controller (MAC) and a SerDes module. Depending on where the MXGXS is instantiated in the data path, the module will be considered a DTE M-XGXS or a PHY M-XGXS. It can support the XAUI interface for incorporation into a customer's own ASIC design.

The M-XGXS module performs all mandatory and optional functionality described in Clause 47 of the IEEE 802.3ae specification. The module is made up of three main sub-modules (as illustrated in the diagram above) and two DDR modules necessary for XGMII traffic. There are many different possible applications for the M-XGXS, including network interface designs, Ethernet switching designs, and test equipment designs.

Major product features:

- Fully compliant with IEEE 802.3ae Clause 47
- Supports 802.3ae Clause 45 MDIO interface
- Tolerance of lane skew up to 16ns (50 UI)
- IEEE 802.3ae PICs compliance matrix
- Verified with third party XAUI cores and SerDes
- Supports 802.3ae Clause 48
- Psuedo random idle insertion
- Clock frequency of 156.25 MHz
- Optional low power mode
- Supports 802.3ae Annex 48A jitter test pattern
- Supports Altera's Stratix GX device family
- Supports lane synchronization
- Supports lane to lane alignment

Deliverables:

- Verilog source code
- Detailed design documentation, including submodules
- Synthesis constraints files
- Functional testbench with documentation
- Wrapper integrating the M-XGXS with Mentor's A-XGMAC core

Related products:

- A-XGMAC™ 10Gbps Ethernet MAC core
- A-XGFIF™ 10Gbps FIFO module
- M-XGPCSR™ 10GBASE-R physical coding sublayer

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Structure

The M-XGXS pack includes the following RTL modules:

- **MXGXS** – *Top-level module*
- **MXGXS_TXCORE** – *XAUI transmit module responsible for 8B/10B encoding, test control implementation, and error reporting*
- **MXGXS_RXCORE** – *XAUI receive module responsible for synchronizing incoming streams to a common clock, lane skew removal, and 8B/10B decoding*
- **MXGXS_MGMT** – *MII management module*
- **MXGXS_DDRIN** – *XGMII double data rate input module*
- **MXGXS_DDROUT** – *XGMII double data rate output module*

Functionality

In transmit direction, the M-XGXS core receives XGMII data and performs idle conversion, code group generation, and 8B/10B encoding. Next, the M-XGXS prepares the data for transmission by a 4-lane SerDes module. In the receive direction, the M-XGXS module accepts 4-lane wide data from a SerDes module and re-aligns it for 8B/10B decoding before passing it out onto an XGMII data bus.

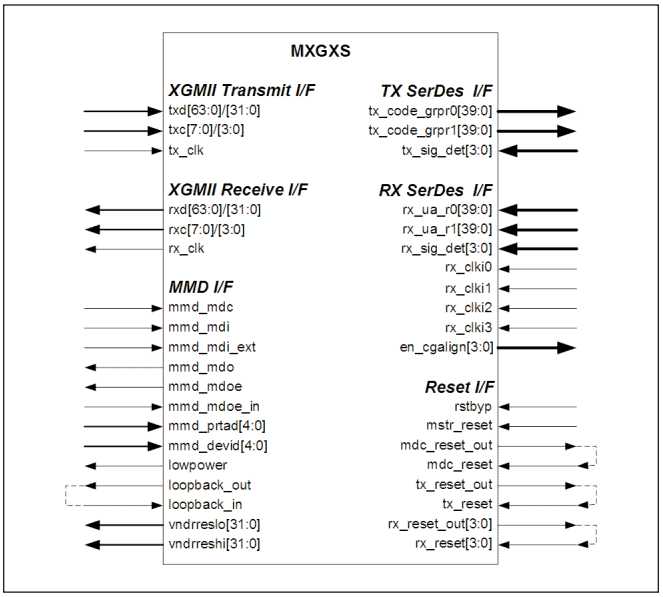
Standards Support

The M-XGXS supports both the IEEE 802.3 Clause 36 and IEEE Clause 802.3ae Clause 45, Clause 47, Clause 48 and Clause 48A specifications.

Tool Flow

The supplied testbenches have been run on different simulator software and different platforms before shipment in order to ensure correct operation at the licensee's facility. Among the tools used: Cadence Verilog NC (native compile), Cadence Verilog (cross compile), and Mentor Graphics ModelSim®. The code has been executed in both UNIX and PC environments.

In addition, the Verilog RTL has been constrained and synthesized by Synopsys Design Compiler using third party standard cell libraries. The libraries were selected to be representative of the current technology at the time of testing. The constraints and design rules used during this process are intended to be generic in nature.



Block Instantiation Diagram

Application

The M-XGXS can be used in many different applications. However, because of its speed, the M-XGXS is best suited for switches, multi-port bridges, and routers.

Reference Technology Gate Count: approx. 43,500 gates

About Mentor Graphics Silicon-Proven, Standards-Based Intellectual Property

Mentor Graphics offers a variety of industry-leading, standards-based IP cores that are rigorously tested and validated to provide design teams with the most reliable cores in the industry. Mentor's IP portfolio ranges from simple SoC building blocks, such as communications interfaces and microcontrollers, to an expansive offering of products for Ethernet, USB, Storage, and PCI Express.

Visit www.mentor.com/ip for more information on our complete IP portfolio of Storage, Ethernet, USB, and PCI Express products.

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Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

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