

PE-MSTAT Application

Overview

The PE-MSTAT is a low gate count, register based, statistics gathering module, developed for integration with the entire Inventra™ range of Ethernet Media Access Controller product families.

The PE-MSTAT has been designed to facilitate easy scaling of counter bit widths, and to allow the module gate count to be decreased for specific MAC applications through complete removal of particular counters. Details of required counter widths and optional counter groups simply need to be specified within the appropriate compile file.

The PE-MSTAT module was designed in Verilog and is provided to licensees with a behavioral testbench.

Major Product Features:

- Designed to integrate with Inventra's Ethernet MAC families
- 37 separate counters
- Supports RMON MIB groups 1, 2, 3 and 9; RMON MIB 2; and dot 3 Ethernet MIB
- Low gate count
- Designed to allow gate count to be further reduced through easy scaling of counter widths or complete removal of counters that are not required
- Fully synthesizable
- Scan insertion-friendly design
- Can be implemented in <0.5µm CMOS

Deliverables:

- Verilog source code
- Synthesis constraints files
- Detailed design specification
- Application Note

Mentor Graphics is the leading supplier of a broad range of IP soft cores targeting standards-based communications applications. These highly re-usable cores help systems and chip designers get to market faster.

PE-MSTAT Statistics Module for Inventra's Ethernet MAC Cores

Operation

During a transmit operation, the selected MAC's Transmit Function module generates a Transmit Statistics Vector, which is automatically updated in response to particular events. The PE-MSTAT module looks at selected bits from the Transmit Statistics Vector whenever the Transmit Statistics Vector Pulse (TSVP) is asserted.

Similarly, during receive operations, the MAC's Receive Function module generates a Receive Statistics Vector which the PE-MSTAT module examines whenever the Receive Statistics Vector Pulse (RSVP) is asserted.

The presence of non-zero elements in either of these statistics vectors triggers PE-MSTAT to update its statistics counters.

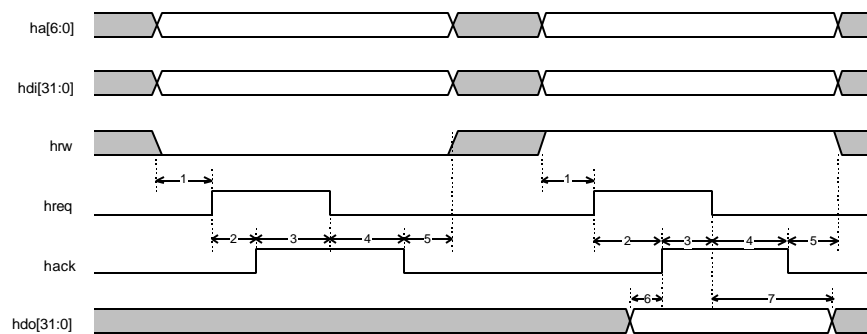
PE-MSTAT is capable of maintaining worst-case throughput conditions of 1 Receive event and/or 1 Transmit event per 4 PE-MSTAT internal clocks.

Counters

The PE-MSTAT module offers 37 separate counters, which can be used either simply to count or to accumulate conditions such as dropped frames that occur as packets are transmitted or received.

The range of counters offered allows support of RMON MIB group 1, group 2 (if table counters), group 3 or group 9; RMON MIB 2; and the dot 3 Ethernet MIB.

Host Interface Timing



If required, roll-over of any of the counters can generate an interrupt. Alternatively internal masking registers may be used to discretely mask each counter's roll-over from causing an interrupt.

Configuration

In general, it is possible to tailor the range of counters in the PE-MSTAT and their widths (and hence the gate count) to the chosen application because the counter widths that are needed depend on the frequency at which the monitored events are expected to happen.

The PE-MSTAT was designed with the intention that, during worst-case stimulation of the PE-MSTAT, the controlling ECU should read each counter at one second intervals. Two monitoring schemes are supported – polling the counters in strict rotation, and responding to interrupts as they occur. If the interrupt scheme is implemented using the PE-MSTAT's Carry signal, a significant decrease can be realized in the aggregate ECU bandwidth required since worst-case conditions only occur rarely.

The factors affecting what counters and counter widths are required are described in an Application Note supplied alongside the PE-MSTAT module. This Application Note also describes some example host service routines.

In addition, a range of logical modules are provided with the PE-MSTAT module, together sample compile files (described in the Application Note). These logical modules

may be used to implement a range of simple incrementors, half-duplex incrementors, incrementors that respond only to transmit errors, and adders of different lengths.

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