

# **MENTOR GRAPHICS**

## ETHERNET IP FAQ

## **What type of solutions does Mentor Graphics offer for 10/100Mbps Ethernet products?**

Besides offering the industries most silicon proven 10/100 Media Access Controller (MAC) with built-in support for the MII interface, Flow Control, and MII Management, Mentor Graphics provides additional solutions for the following:

- PHY Interfaces: RMII, SMII, ENDEC, PMD
- CPU Interfaces w/o buffers: Generic Asynchronous/Synchronous with chip select
- CPU Interfaces w/ buffers: AHB, Generic Request/Acknowledge Handshaking
- Data Buffering: cut-thru or store and forward operations
- Filtering: up to 16 different criteria plus address based filtering
- Statistics: Various RMON, SNMP, or custom defined counters

## **What type of solutions does Mentor Graphics offer for Gigabit Ethernet products?**

Besides offering the industries most silicon proven 10/100/1000 Mbps Media Access Controller (MAC) with built-in support for the G/MII interface, Flow Control, and MII Management, Mentor Graphics provides additional solutions for the following:

- PHY Interfaces: RMII, RGMII, SMII, SGMII, 10-bit SERDES (PCS)
- CPU Interfaces w/o buffers: Generic Asynchronous/Synchronous with chip select
- CPU Interfaces w/ buffers: AHB, Generic Request/Acknowledge Handshaking
- Data Buffering: cut-thru or store and forward operations
- Filtering: up to 16 different criteria plus address based filtering
- Statistics: Various RMON, SNMP, or custom defined counters
- Wake-On-LAN support

## **What type of solutions does Mentor Graphics offer for 10-Gigabit Ethernet products?**

Besides offering a multi-process silicon proven 10-Gigabit Media Access Controller (MAC) with built-in support for the XGMII interface, OC-192 support, Flow Control, and MII Management, Mentor Graphics provides additional solutions for the following:

- PHY Interfaces: XAUI, XSBI (64/66b PCS layer)
- CPU Interfaces w/o buffers: Generic Asynchronous/Synchronous with chip select
- CPU Interfaces w/ buffers: Generic Request/Acknowledge Handshaking
- Data Buffering: cut-thru or store and forward operations
- Filtering: up to 16 different criteria plus address based filtering
- Statistics: Various RMON, SNMP, or custom defined counters

## **Does Mentor Graphics support FPGA versions of the Ethernet cores?**

The PE-MACMII (10/100 Ethernet MAC core) and PE-MCXMAC (10/100/1000 Ethernet MAC core) and their supporting modules are currently available as open source or encrypted RTL format for Altera FPGAs. These cores when licensed as open source can be implemented in both Altera and Xilinx FPGAs without any RTL modifications. The A-XGMAC core offers a more gate heavy design option that allows for FPGA implementation in certain Altera device

families. Device family support is limited to devices with enough chip resources for the Ethernet cores to achieve the necessary timing and I/O requirements.

For Xilinx device support in netlist format Mentor Graphics has partnered with Memec Design ([www.memec.com](http://www.memec.com)) to offer our Ethernet cores as encrypted source or netlists for Xilinx's family of FPGAs. Customers interested in a Xilinx only solution should contact Memec directly for device availability.

### **What deliverables are included in Mentor Graphics Ethernet cores?**

The Ethernet core deliverables with the purchase of RTL source code include the following:

- Synthesizable Verilog RTL source code
- Functional test bench
- Modular level documentation
- Synopsis constraint files for synthesis scripts
- Annual Support and Maintenance service available after initial support period expires.

### **Does Mentor Graphics offer any Ethernet cores in VHDL?**

Mentor Graphics does not currently offer any cores in VHDL. However, Mentor Graphics does provide VHDL wrappers for instantiating the Ethernet cores in a mixed coding environment.

### **What design rules does Mentor Graphics use when coding their IP?**

Mentor Graphics Ethernet cores comply with the Verilog RTL coding "RULES" and "GUIDELINES" for soft-core macros, as defined in the "Reuse Methodology Manual" second edition, with a few intentional exceptions. All Mentor Graphic Ethernet Verilog RTL is evaluated by industry leading linting tools.

### **Do the Ethernet MAC cores contain multiple clock domains or any negative edge flip-flops?**

All of the Mentor Graphic Ethernet cores use a one clock, one edge design approach for each sub-module within the core. The only exception is the clock and reset module, which handles any necessary clock division and reset synchronization logic.

The only time a negative clock edge is used is when the Ethernet specification being implemented calls for the use of a negative clock edge. All negative edge clocking is isolated to a single sub-module and converted to positive edge clocking as soon as possible (receive path) or as late as possible in the data path (transmit path).