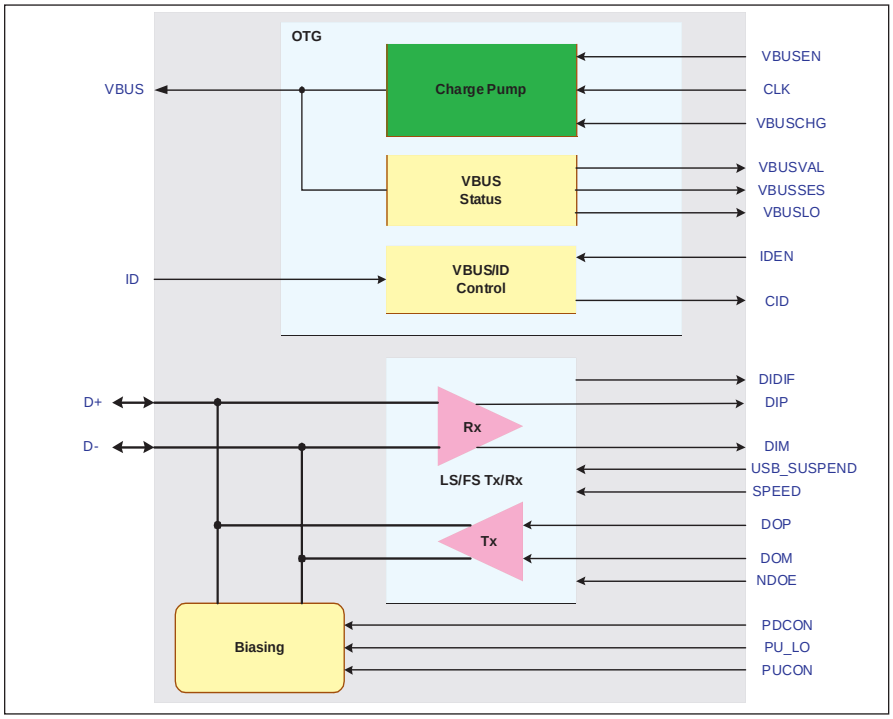
USB 2.0 PHY IP

Full-Speed USB PHY

MUSBFPHY

D A T A S H E E T



MUSBFPHY block diagram.

Full-Speed USB PHY

The MUSBFPHY IP PHY from Mentor Graphics® is an on-chip transceiver for USB On-The-Go (OTG) that complies with both the USB standard for Full-Speed functions and the OTG supplement to the USB 2.0 specifications. It is capable of transmitting and receiving serial data at both Full-Speed (12Mbit/s) and Low-Speed (1.5Mbps), providing low-cost connectivity for consumer portable devices such as mobile phones, PDAs, digital still cameras, and MP3 players.

MUSBFPHY interfaces directly with the MUSBFDRC Full-Speed dual-role controller to create a complete System-on-Chip (SoC) solution for USB. An on-chip charge pump provides power for the USB directly from the SoC without the need for an external 5V power supply.

Mentor designed this IP PHY for low power consumption, minimal die area, and high-data throughput. When implemented in the TSMC .13G standard, the MUSBFPHY provides a complete on-chip transceiver package with ESD protection, charge pump, and support for OTG-specific features like Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) in just 1.36mm^2 of die area.

Finally, with the combination of embedded software stack, device drivers, and dual-role link controllers (MUSBMHDRC and MUSBFPHY), Mentor Graphics is in the unique position of providing a complete and fully integrated IP hardware/software solution for Full-Speed USB OTG.

Major product features:

- Fully compliant with USB 1.1 and 2.0 Full-Speed and OTG standards
- Supports Full-Speed (12Mbps) and Low-Speed (1.5Mbps) serial data transmission
- Built-in charge pump
- Dual 3.3V/1.2V supply
- 80mA driving current with 528mW power dissipation at maximum load
- Uses digital inputs and outputs to transmit and receive USB data
- Supports single-ended data receives
- Includes VBus short-circuit protection
- Can be ported to any standard CMOS-based fabrication process
- Supports all popular platforms including Mentor's ModelSim® and Questa™ co-verification environments
- 40um staggered bond pitch
- 40MHz input clock required

Deliverables:

- Flattened Spice netlist
- Verilog simulation model
- Process-specific specification
- Integration, layout, & test guides
- LVS & DRC check reports
- Place-and-route views: (.lib, .lef, and antenna.lef)
- GDSII layout & layout map

Related products:

- **MUSBHPHY** - USB High-Speed PHY
- **MUSBMHDRC** - USB 2.0 High/Full-Speed OTG controller
- **MUSBFDRC** - USB 2.0 Full-Speed OTG controller
- **MUSBHSFC** - USB 2.0 High/Full-Speed function controller

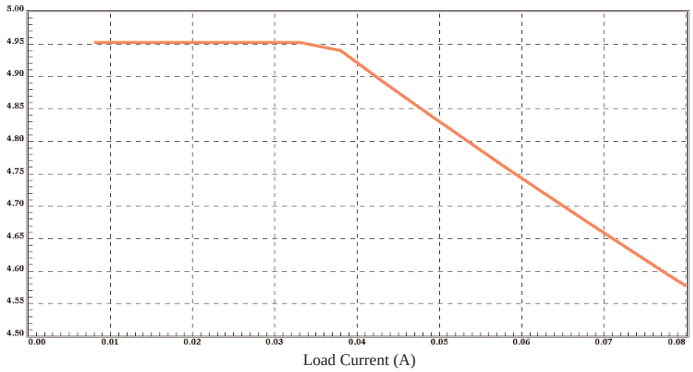
Mentor Graphics®

Built-in Charge Pump

The design includes a built-in charge pump that achieves a VBus output voltage of 4.95V with load currents between 8mA and 40mA, as shown in the diagram at right.

The charge pump circuit requires four pins and two external capacitors.

Regulation Range at Different Load Currents (Typical Values)



Signal Description

Signal	Type	Description
USB INTERFACE		
D+, D–	A-IO	USB standard differential data bus.
ID	A-IO	USB plug indicator.
VBus	Power	USB power line.
CHARGE PUMP CONNECTIONS		
CLK	Input	Input clock for charge pump (48MHz)
OUT1B/2B	Power	Connections to capacitors – see Block Diagram.
IC1, IC2	Power	
FUNCTION CONTROLLER INTERFACE		
DIP	Output	D+ single-ended input to controller.
DIM	Output	D– single-ended input to controller.
DIDIF	Output	Output from Differential Input Receiver.
DOP	Input	D+ output from controller.
DOM	Input	D– output from controller.
NDOE	Input	Enable for DOP, DOM (active low).
SPEED	Input	Transceiver operating speed: 1=full-speed, 0=low-speed.
USB_ SUSPEND	Input	Indicates when the connected OTG device is in Suspend mode.
PUCON	Input	Selector for pull-up resistor on D+.
PU_LO	Input	Control of pull-up resistor value.
PDCON	Input	Selector for pull-down resistor on D+.
VBUSEN	Input	VBus power enable (controller = ‘A’ device).
VBUSCHG	Input	Charge VBus signal (used in SRP when controller = ‘B’ device).
VBUSVAL	Output	VBus compared to selected VBus Valid threshold.
VBUSSES	Output	VBus compared to ‘B’ Session Valid threshold.
VBUSLO	Output	VBus compared to Session End threshold.
CID	Output	MUSBFDRC Connector ID.
IDEN	Input	Enable signal for sampling ID.

Power Consumption

Parameter	Condition	Max Power Consumption
Charge Pump Power	Typical Max Load (80mA) Worse Case Max Load (40mA)	528mW
Driver	Full Speed	11.5mW
	Low Speed	9.7mW
Buffer	Full Speed	2.0mW
Comparators		5.5mW

Portability

The MUSBFPHY is designed for portability. The core’s fully CMOS-based implementation can be readily re-targeted to any foundry process in use today.

The port to a customer’s required technology will be carried out within Mentor Graphics as part of the delivery process.

Visit www.mentor.com/ip for additional IP product information.

© 2006 Mentor Graphics Corporation. All Rights Reserved.
Questa is a trademark and ModelSim and Mentor Graphics are registered trademarks of Mentor Graphics Corporation. All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
Fax: 503-685-1204
Sales and Product Information
Phone: 800-547-3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501
North American Support Center
Phone: 800-547-4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140 0001
Japan
Phone: 81-3-5488-3033
Fax: 81-3-5488-3004

MGC-10/06 1025360-w