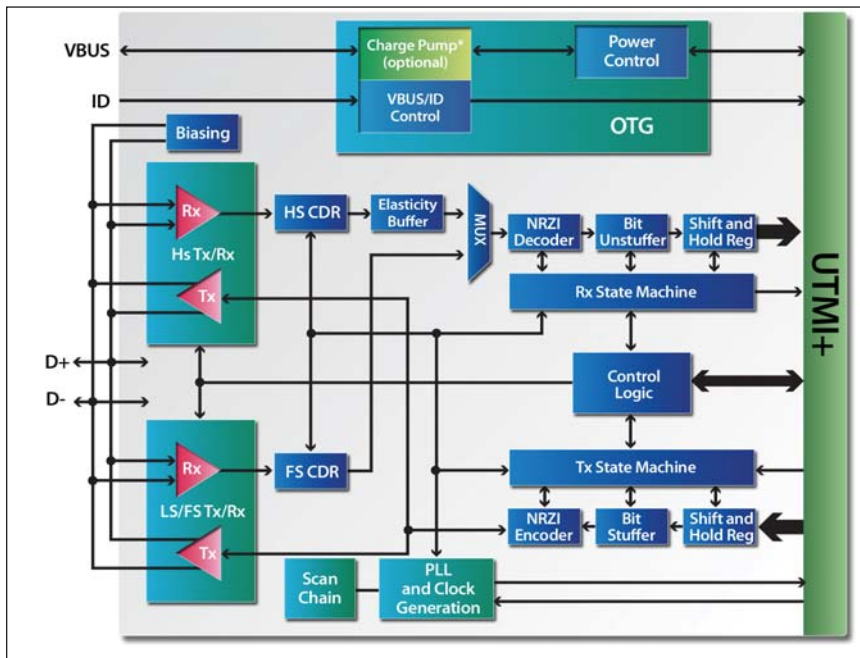


# USB 2.0 PHY IP

## Hi-Speed USB UTMI+ PHY

## MUSBHPHY

## D A T A S H E E T



UTMI+ PHY block diagram.

## Hi-Speed USB PHY

MUSBHPHY from Mentor Graphics® is a Hi-Speed USB 2.0 transceiver for use with host, embedded host, On-The-Go (OTG), and function controllers. Compliant with the UTMI+ level 3 (USB 2.0 Transceiver Macrocell Interface Plus) specification, the MUSBHPHY integrates Hi-Speed, mixed-signal circuits to support Hi-Speed traffic at 480Mbps and is backward compatible to Full-Speed (12Mbps) and Low-Speed (1.5Mbps) data rates.

This transceiver is optimized for low power consumption, minimal die area (sub-1mm<sup>2</sup>), and high-data throughput. The MUSBHPHY comprises a complete on-chip physical transceiver solution with Electro Static Discharge (ESD) protection, full support for OTG and host functionality, and includes an optional charge pump to provide a 5V power supply to external USB peripherals.

The MUSBHPHY includes a clock generation block with a PLL unit to ensure accurate Hi-Speed data transmission from and to the transceiver. The MUSBHPHY requires a 12MHz reference clock input to the PLL unit.

The transceiver is available for the SMIC 130 nm standard digital process. Contact Mentor Graphics for information on supported processes. Samples of MUSBHPHY have been integrated into Mentor reference platforms for interoperability testing and validation of USB standard compliance.

## Major product features:

- Fully compliant with USB 1.1 and 2.0
- Supports Hi-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps)
- Supports peripheral, host, embedded host, OTG, and hub applications
- Dual 3.3V/1.2V supply
- Rail-to-rail common mode differential receiver
- Digital I/O for Tx & Rx USB OTG cable type
- 40um staggered bond pitch
- Optional charge pump 100mA supply current at 4.4V Vbus under typical conditions
- Supports all popular platforms including Mentor's ModelSim® and Questa™ verification environments
- No external 5V supply needed
- Scan-based DFT and loop back
- ESD and analog I/O structure included
- GDSII available in 6, 7, and 8 metal layer options

## Deliverables:

- GDSII layout & layer map
- Place-and-route views (.lib, .lef)
- LVS & DRC verification reports
- Verilog Sim Model (NC-Verilog)
- Gate-level netlist & SDF timing
- Test guidelines, layout guidelines, and application notes

## Related products:

- **MUSBFPHY** - USB Full-Speed PHY
- **MUSBMHDR** - USB 2.0 Hi/Full-Speed embedded host OTG controller
- **MUSBFDRC** - USB 2.0 Full-Speed embedded host OTG controller
- **MUSBHSFC** - USB 2.0 Hi/Full-Speed function controller
- **MUSB-MicroSW** - USB software stack, supports all Mentor USB controllers

## Signal Description

|   | SIGNALS                       | TYPE   | DESCRIPTION                                 |
|---|-------------------------------|--|---|
| USB                                     | DP/DM                         | A - I/O  | USB Standard Differential Data Bus          |
|   | ID                            | A - I/O  | USB Plug Indicator                          |
|   | VBUS                          | Power  | USB Power Line                              |
| Charge Pump Interface                   | IC1/ IC2                      | I/O  | External Capacitor Connection               |
|   | OUT1B/ OUT2B                  | I/O  | External Capacitor connection               |
|   | CP_XCTRL                      | D-In   | Charge Pump Enable/Disable                  |
|   | DrvVBus                       | D-In   | Charge Pump Enable UTMI Control             |
| PLL Bias                                | FREF                          | I/O  | 12Mhz Crystal Input                         |
|   | REXT                          | A - I/O  | 12.4Kohm Reference External Resistor        |
| UTMI                                    | DataIn[7:0]/DataOut[7:0]      | I/O  | 8-Bit Parallel I/O Data Bus @ 60Mhz         |
|   | TxValid / TxReady             | I/O  | Transmit Data Valid and Ready               |
|   | RxActive / RxValid / RxError  | D-Out  | Receive Data Active, Valid and Error        |
|   | Reset / SuspendM              | D-In   | Reset and Suspend Mode Enable               |
|   | TermSelect                    | D-In   | Termination Select between FS/LS & H/S      |
|   | XcvrSelect[1] / XcvrSelect[0] | D-In   | Transceiver Select between FS/LS & H/S      |
|   | OpMode[1] / OpMode[0]         | D-In   | Operational Mode Selector                   |
|   | LineState[1] / LineState[0]   | D-out  | USB Bus Line State Monitor                  |
|   | CLK                           | D-Out  | 60Mhz Output Clock                          |
|   | UTMI+                         | IDPullUp   | D-In  |
| IDdig                                   |                               | D-Out  | USB Plug Indicator Out                      |
| AValid / BValid / VBusValid / SessValid |                               | D-Out  | A, B, VBus, Session valid Comparator output |
| ChrgVbus / DisChrgVBUS                  |                               | D-In   | VBus Charge and Discharge Enable            |
| HostDisconnect                          |                               | D-Out  | Peripheral Disconnection indicator          |
| DpPulldown / DmPulldown                 |                               | D-In   | D+ and D- Pull Down Resistor Enable         |
| TxBitStuffEnable                        |                               | D-In   | Enable Bit Stuffing when OPMODE is 11       |
| FsLsSerialMode                          |                               | D-In   | Enable Communication w/ USB 1.1 Controller  |
| Tx_Enable_N                             |                               | D-In   | Active Low Output Enable                    |
| Tx_DAT / Tx_SE0                         |                               | D-In   | Differential Data or Single Ended           |
| Rx_RCV / Rx_DP / Rx_DM                  | D-Out                         | Receive Differential or Single DP / DM at 12Mbps |   |
| Test <sup>1</sup>                       | scan_reset                    | D-In   | Reset the Scan Flops Within the PHY         |
|   | CLK1                          | D-In   | First Test Clock                            |
|   | CLK2                          | D-In   | Second Test Clock                           |
|   | Scan_set                      | D-In   | Scan Flops Set Active High                  |
|   | Test_en                       | D-In   | Scan Test Enable Signal Active High         |
|   | Loop_Back                     | D-In   | Loop Back Test Enable Signal Active High    |
|   | Scan_en                       | D-In   | Scan Flops Shift Enable Signal Active High  |
| Supply                                  | 1.2V / 3.3V                   | Power  | Power Supply Requirement Analog and Digital |

1: Scan inputs and outputs are shared with DataIn[4:1] and DataOut[4:1] respectively.

## Built-in Charge Pump

The design includes an optional built-in charge pump that achieves a Vbus output voltage of 4.95V with load currents up to 110mA in typical conditions. The charge pump circuit uses two non-overlapping clocks generated from the internal clock generation block to charge two external 1uF capacitors.

### Power Consumption

**Rx mode - 57mW**

**Tx mode - 42mW**

### Charge Pump

**Typical Max Load 110mA**

**Worst Case Max Load 80mA**

### MUSBPHY Availability

*MUSB-PHYC - S13A - With Charge Pump*

*MUSB-PHYN - S13A - Without Charge Pump*



Visit [www.mentor.com/ip](http://www.mentor.com/ip) for additional IP product information.

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