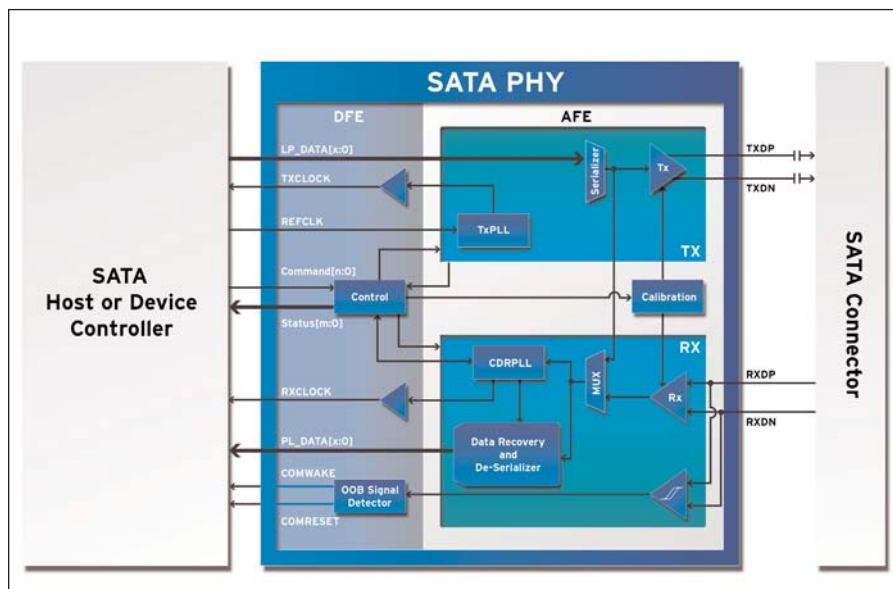


# MSATA\_PHY

## Serial ATA 1.5/3.0 Gbps PHY IP Core

MSATA\_PHY

D A T A S H E E T



The MSATA\_PHY block diagram from Mentor Graphics.

### Mentor's Complete Serial ATA Hardware Solution

The Mentor Graphics® MSATA\_PHY core provides PHY layer functionality for a Serial ATA (SATA) interface operating at 3Gbps or 1.5Gbps. The MSATA\_PHY core contains all the analog/mixed-signal components required to implement the industry standard SATA protocol within the physical layer and when combined with Mentor Graphics SATA Host or Device controller, the core provides a complete SATA hardware solution. The IP components include: transmitter drivers, receiver input buffers, impedance matching circuitry, amplitude and impedance calibration circuitry, parallel-to-serial and serial-to-parallel converters (serializer/deserializer), clock tuning & alignment mechanisms, OOB signal detection, clock speed & parallel bus width selection, test modes, and power management.

The MSATA\_PHY core is configured for a single channel SATA connection, interfacing as a point-to-point connection to another SATA physical layer such as SATA disk drive at serial data rates of 3Gbps or 1.5Gbps. The IP core also connects to the SATA link layer implementing the SATA specification defined PHY interface via a parallel data bus with the appropriate clock speeds for either a 3Gbps configuration or a 1.5Gbps configuration. When used with Mentor's SATA Host and Device controllers, the MSATA\_PHY core implements a 20-bit parallel interface running at 150 MHz for 3Gbps or 75 MHz for 1.5Gbps operation. The MSATA\_PHY core includes power management, impedance calibration, and test modes such as loopback and BIST.

### Major product features:

- Includes support for the following processes:
  - TSMC 130nm LVOD
  - SMIC 130nm G
- Compliant to the Serial ATA specification
- Selectable 1.5 Gbps or 3.0 Gbps high-speed serial data communication
- Supports hot swapping
- Configurable 40-, 20-, or 10-bit parallel controller interface
- Analog portion front-end (AFE) resides inside IO pad ring occupying zero core area
- All required Power Pads are contained within the core, all pins connected to external pads
- Consumes less than 80mW (including termination power)

### Deliverables:

- Verilog behavioral simulation model (NC-Verilog)
- Integration and test guidelines
- Application notes

### DFE-Specific Deliverables:

- Synthesizable Verilog RTL code
- Example synthesis scripts
- Synthesis and static timing analysis reports

### AFE-Specific Deliverables:

- GDSII layout and layer map
- Place and Route LIB & LEF views
- LVS and DRC verification reports

### Related products:

- **Serial ATA IP** - Host Controller
- **Serial ATA IP** - Device Controller with optional integrated DMA

## Functional Specifications

The MSATA\_PHY core is subdivided into two main blocks:

- Analog Front End - AFE Block
- Digital Front End - DFE Block

The associated functional blocks are shown in the diagram on the front of this datasheet. The AFE block is subdivided into 3 blocks consisting of Transmitter - Tx, Receiver - Rx, and Control/Test submodules. The DFE block is subdivided into 3 blocks consisting of Control Logic, Clock Repeaters, and OOB Signal/Detector submodules.

The Transmitter submodule in the AFE block receives encoded data from the DFE block synchronous with TXCLOCK generated in the Tx sub-block, and serializes the data for transmission over the SATA connector. The Receiver module in the AFE block receives the serialized data from the SATA connector, de-serializes the data into parallel data and recovers the Receive clock, RXCLOCK, before sending the

data to the DFE block. The Control/Test submodule in the AFE block performs the calibration functions, power management functions, and test mode functions such as loopback and BIST per the instructions provided by the DFE block.

The Control Logic submodule in the DFE block receives the SATA Controller Command instruction set, executes them accordingly, and issues instructions to the AFE block. Similarly, the Control Logic submodule receives status information from the AFE block and when appropriate, reports the status to the SATA controller. The Clock Repeaters submodule buffers and transmits the clocks generated in the AFE block to the SATA controller. The OOB signal detector submodule decodes the “Out of Band” signal generated in the AFE block, and provides reset signaling, initialization, or speed negotiation. This block also observes the presence or absence of the received signal in a predetermined chirp pattern.

## I/O Description:

Signal	Type	Description
REFCLK	Input	Reference System Clock at 150Mhz
TXCLOCK	Output	Parallel interface Transmit data clock. Generated from the Tx PLL
RXCLOCK	Output	Recovered Parallel interface Receive data clock. Generated from the Rx PLL
TXDP, TXDN	Output	Differential Serialized Transmit data output to the P HY
LP_DATA[x:0]	Input	Parallel data input bus from the Link Layer, where x = 39, 19, or 9 depending on configuration setting.
RXDP, RXDN	Input	Differential Serialized Receive data from the PHY
PL_DATA[x:0]	Output	Parallel data output bus to the Link Layer, where x = 39, 19, or 9 depending on configuration setting
COMMAND SIGNALS [n:0]	Input	Command interface signals from the Link Layer, includes speed selection, power modes, data width, PHY type, loopback, and test modes.
STATUS SIGNALS [m:0]	Output	Status interface signals to the Link Layer, includes speed indication, comma detect, PHY status, and errors
COMWAKE	Output	Signal from OOB detector, indicates ComWake detection
COMRESET/COMINIT	Output	Signal from OOB detector, indicates ComReset for device and ComInit for Host

## Reference Technology Gate Count:

- Per lane size of <0.3mm<sup>2</sup>
- 40um staggered bond pitch
- DFE gate count:
  - 16,000 (TSMC 130nm LVOD)
  - 9,000 (SMIC 130nm G)

Visit our website at [www.mentor.com/ip](http://www.mentor.com/ip) for additional product information.

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