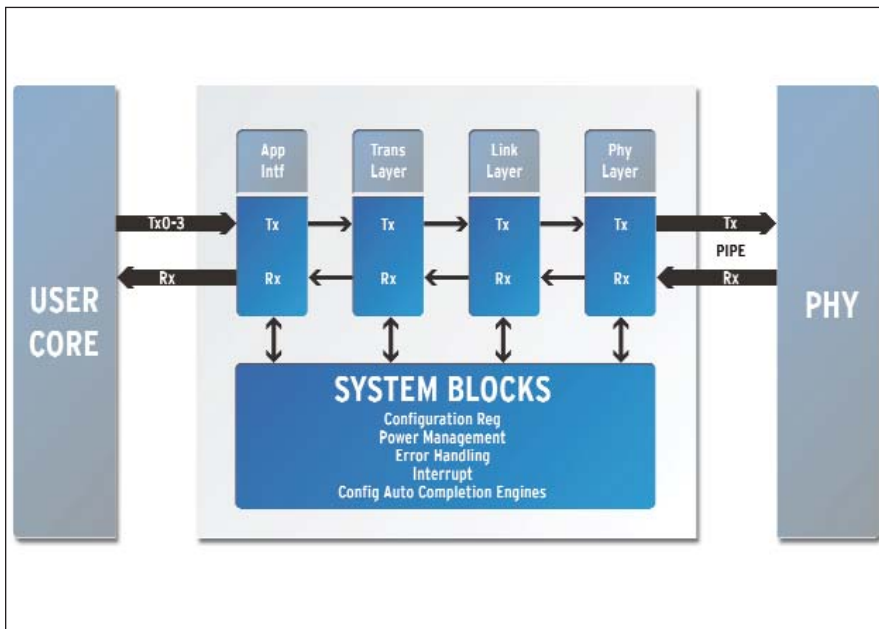


# PCI Express® Product Family

Includes: x1, x2, x4, x8 and x16 Controllers

Digital Controller IP

D A T A S H E E T



The Mentor Graphics PCI Express® controller is PCI-SIG® 1.1 compliant and can be easily tailored to both ASIC and SoC designs.

"Doing more for less" drives the adoption of any new technology. PCI Express (PCIe) is no exception. In reality, increasing I/O bandwidth and decreasing real estate requirements have necessitated the adoption of PCIe technology throughout many of today's most popular applications.

The complete line of PCIe controller IP from Mentor Graphics® is silicon-proven, highly configurable, and ready to meet the most rigorous design challenges. These scalable controllers are PCI-SIG 1.1 compliant and can be tailored toward specific market segments including ASIC and SoC designs. For example, controllers with up to 4-lanes (x4) are best suited for wireless, mobile, consumer, communication, and embedded markets. The attributes needed for this market include low gate count, low power, active state power management, and low latency. Controllers with 8-lanes (x8) or 16-lanes (x16) are more suitable for storage, graphics, and server back-end applications. Regardless of application, design teams require the end-to-end and internal data integrity protection that the Mentor Graphics PCIe controller solution provides.

## Major product features:

- Product family: x1, x2, x4, x8, x16 controllers
- PCIe® specification 1.1 compliant
- Each controller is fully optimized for minimum gate count
- Each controller can be configured for: Endpoint, Root Port, Dual (Endpoint/Root), or Switch Port mode
- Optional legacy mode support
- Multi-function support up to 8 functions
- Multi-VC support up to 8 channels
- Capable of queuing up to 8 transactions concurrently
- High-performance with low latency and maximum throughput
- Low silicon footprint - suitable for multiple instances of the core in single ASIC/FPGA
- Highly parameterized core supporting both cut-through and store-and-forward schemes
- Supports operation with 8-bit and 16-bit PIPE interface
- Implements optional configuration space and capability structures
- Configurable retry buffering scheme for low footprint and latency
- Supports all power management states L0, L0s, L1, L2, and L3
- Supports beacon and wake-up mechanism from deep sleep states
- Clock request (ClkReq) mechanism for low power mode in mobile form factors
- Supports PCIe advanced error reporting

## Deliverables:

- Synthesizable Verilog RTL
- Sample testbench for simulation
- Sample synthesis scripts
- Sample static timing analysis
- Documentation

## Architected by Industry Veterans

The PCIe controller IP family from Mentor Graphics has highly configurable and scalable architecture for design flexibility. Each controller IP is fully optimized to reach low gate count and high throughput. With multiple datapath widths, the PCIe IP core offers maximum performance based on the specific lane width requirements. The PCIe controller IP family includes multi-function support (up to eight functions) and multi-VC support with up to 8 channels. These PCIe controllers also feature full isochronous traffic support with multiple pipelined memory read/write capability. Integration flexibility is further achieved with PIPE logic.

Design for test (DFT) and design for debugability (DFD) features are also built in to the architecture of these PCIe controllers along with a technology independent design that makes them ideal for both ASIC and FPGA systems. A highly configurable retry buffer design is available for low latency and area depending on the user application.

Additional performance features architected into these cores include: very low transmit and receive latency, minimal silicon footprint, non-blocking architecture, maximum PCIe link utilization, and complete low power management support.

## Parameterized Core

These PCIe controller cores offer highly parameterized RTL for easy configurability — depending on requirements. They support both cut-through and store-and-forward schemes when forwarding transmitted packets. All of the multi-lane controllers operate at all possible

NUMBER OF LANES	APPLICATION DATAPATH WIDTH	PIPE PHY WIDTH	PCIe CLOCK FREQUENCY	APPLICATION CONFIGURATIONS	PCIe LINE BANDWIDTH
X1	32 bit	16 bit	125 MHz	Endpoint, Root, Switch, Dual Mode (E/R)	*5 Gbps
X2	64 bit	16 bit	125 MHz	Endpoint, Root, Switch, Dual Mode (E/R)	*10 Gbps
X4	64 bit	16 bit	125 MHz	Endpoint, Root, Switch, Dual Mode (E/R)	*20 Gbps
X8	64 bit	8 bit	250 MHz	Endpoint, Root, Switch, Dual Mode (E/R)	*40 Gbps
X16	128 bit	8 bit	250 MHz	Endpoint, Root, Switch, Dual Mode (E/R)	*80 Gbps

Supported PCIe Controllers with their Respective Configurations

\*Indicates the theoretical maximum line bandwidth.

allowable speeds down to x1 mode. Selectable ECRC and advanced error reporting support are also built in to these IP cores along with configurable Type-0 (Endpoint) or Type-1 (Root Port, Switch Port) configuration headers.

## Plug-and-Play Application Interface

The easy-to-integrate interface with user logic offers controllability for critical device parameters. The streamlined user interface provides a reasonable number of interface signals.

## PCIe Application Configurations

- **Endpoint:** All PCI-based products upgrading to PCIe and all device applications require PCIe controller in Endpoint mode
- **Root Port:** All host applications require PCIe controller in Root Port mode
- **Dual Mode:** Embedded applications needing PCIe for inter-chip communication require PCIe controller in Dual mode — Root Port or Endpoint at power-up
- **Switch Port:** All applications needing more than one PCIe Port require PCIe controller in Switch Port mode

## Silicon-Proven and Reliable



In addition to offering DFT and DFD capabilities, these PCIe controllers have been thoroughly tested and verified against industry-leading PCIe verification suites. Moreover,

the core has passed compliance testing and has been added to the PCI-SIG PCIe Integrators List. Mentor is part of an extensive list of interoperable PCIe vendors.

Visit [www.mentor.com/ip](http://www.mentor.com/ip) for additional PCIe to AMBA 3 AXI/AMBA 2 AHB Bridge and other IP product information.

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