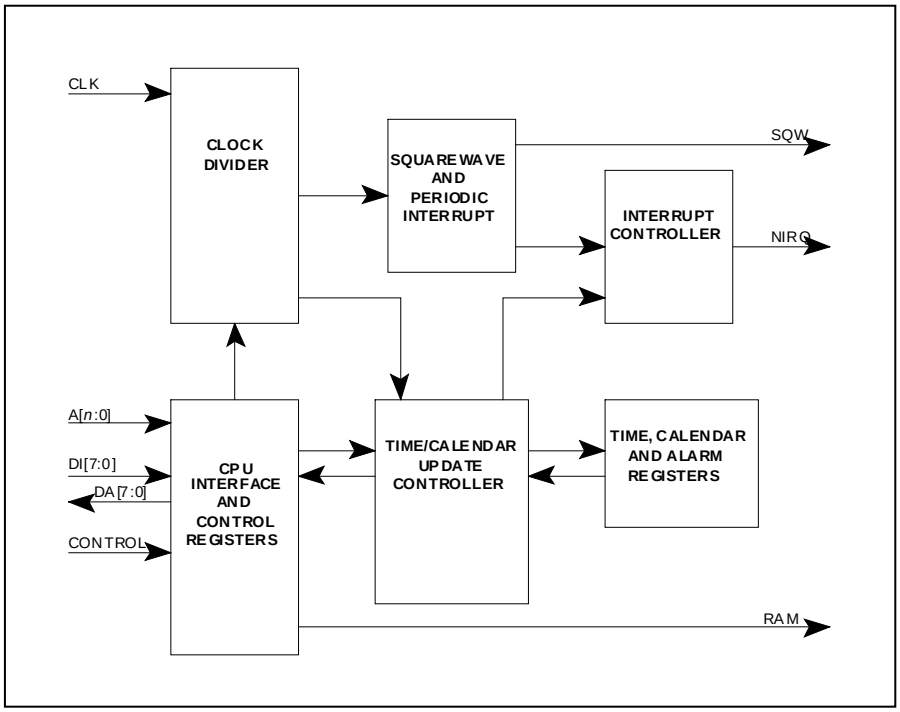
M146818
Real Time Clock

Soft Core (RTL IP)

D A T A S H E E T



M146818 Block Diagram

Overview

The M146818 combines a complete time-of-day clock with an alarm, a 100-year calendar, a programmable periodic interrupt, and a square wave generator. The time can be in 12 or 24 hour mode, and time/calendar values can be stored in binary or binary-coded decimal format. A daylight saving time option is available.

The time-of-day, alarm and calendar registers can all be accessed by an 8-bit CPU bus, and RAM enable signal and address lines are provided to allow a RAM block to be connected. The size of this RAM block is user-definable.

The M146818 has been designed for very low power consumption.

Major Product Features:

- Software compatible with Motorola MC146818
- Ultra low power consumption
- One hundred year calendar
- Programmable periodic interrupt
- Square wave generator
- Interface for connecting to a user-defined quantity of RAM
- Fully synthesizable

Deliverables:

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL testbenches
- Reference technology netlist
- Product Specification & User Guide

Operation

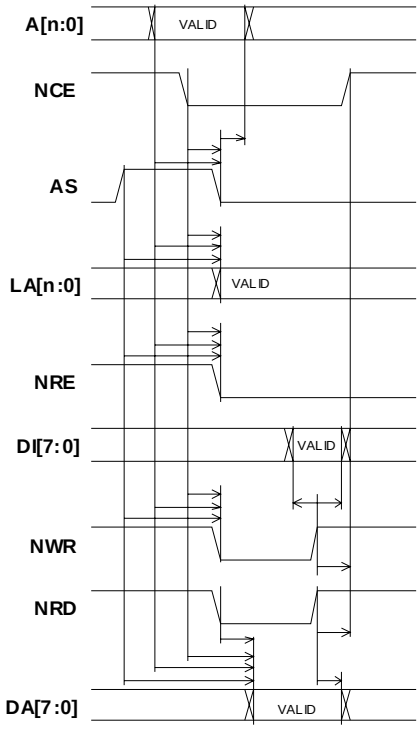
The M146818 contains three time-of-day registers, three alarm registers and four calendar registers which are accessible by an 8-bit CPU bus. It also contains a clock divider which can be driven from a 32768, 1048576 or 4194304 Hz clock.

Once per second, the time and calendar registers are automatically updated. When the time-of-day registers match the alarm registers, an alarm is flagged which can then be used to generate an interrupt. The device can also be programmed to produce a periodic interrupt.

The M146818 decodes a user-settable number of address lines. The first 14 locations are mapped to 14 internal registers: the remaining locations are mapped to an external RAM block, address lines for which are provided within the M146818 – together with a RAM enable signal.

If a crystal oscillator is required, a suitable oscillator cell can be attached outside the M146818.

Timing Information



Signal Description

The M146818 has 16 inputs and 12 outputs, plus a user-definable number of address lines.

SIGNAL	TYPE	DESCRIPTION
CLK	Input	Clock, either 4.194304 MHz, 1.048576 MHz or 32768 Hz
NRST	Input	Reset, active low. Clears interrupt enables: PIE, AIE, UIE, interrupt flags: PF, AF, UF, IRQF and square wave enable SQWE.
A[*n*:0]	Input	Address lines
AS	Input	Address strobe, latches A[*n* –0] when low
LA[*n*:0]	Output	Latched address lines. Can be used to address an external RAM block.
DI[7:0]	Input	Data bus
DA[7:0]	Output	Data bus
NDOE	Output	Data bus output enable, active low. Can be used to control external bidirectional buffers.
NWR	Input	Write strobe, active low
NRD	Input	Read strobe, active low
NCE	Input	Chip enable, active low
NRE	Output	External RAM enable, active low. This signal is low when NCE is low and none of the 14 internal registers are addressed.
NIRQ	Output	Interrupt request, active low
SQW	Output	Square wave output
NMR	Input	Master reset, active low
NTST	Input	Test mode enable, active low

Update Cycle

The time, calendar and alarm registers are updated once a second. Accessing any of these registers during the update cycle will produce undefined results.

The M146818 has three features that can be used to avoid accessing these registers during an update cycle.

One is an ‘Update in progress’ bit which goes high 244µs before the next update cycle. Another is an ‘Update ended’ interrupt which can be set to trigger 998ms before the next update. The third is the periodic interrupt which the device can be programmed to provide. The time available to read the registers after an interrupt has occurred can then be deduced from the periodic interrupt rate.

Reference Technology Gate Count: 2000

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