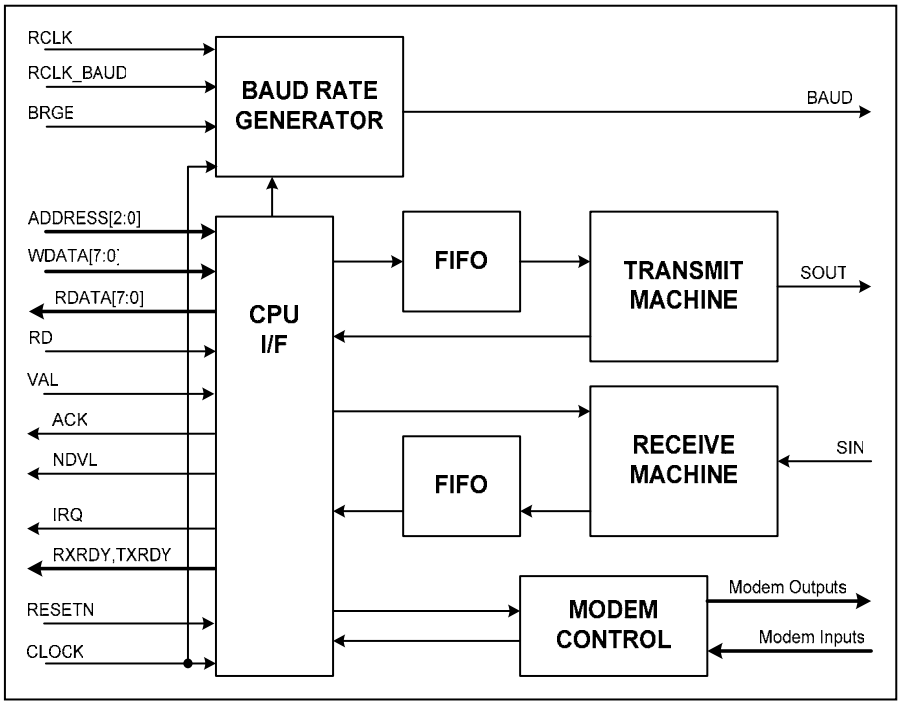
Inventra™ M16x50
Enhanced UART with FIFOs & IrDA Support

Soft Core (RTL IP)

D A T A S H E E T



M16x50 Block Diagram

Overview

The M16x50 is an extension of the Inventra M16550S UART with FIFOs, with enhancements that emulate features found in similar discrete devices with a range of part numbers. Some of the enhancements are enabled by software and are always present in the design: some – such as maximum FIFO size – are configurable and are selected on compilation.

Like the M16550S, the M16x50 offers programmable word length (from five to eight bits), together with an optional parity bit and 1, 1½ or 2 stop bits. If enabled, the parity can be odd, even or forced to a defined state.

Also like the M16550S, the M16x50 includes a 16-bit programmable baud rate generator, an 8-bit scratch register and two DMA handshake lines, TXRDY and RXRDY, which are used to indicate when the FIFOs are ready to transfer data to the CPU. Further, the DMA handshake lines may be configured either to support single-byte transfers (DMA Mode 0) or multiple-byte transfers (DMA Mode 1).

The M16x50 also includes eight modem control lines and a diagnostic loop-back mode. Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

Major Product Features:

- Software compatible with 16C450- and 16550A-compatible UARTs
- Hardware & Software Flow Control
- IrDA Modulation/Demodulation
- Transmit FIFO Threshold
- Configurable FIFO Depth
- CTS and RTS Interrupts
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Diagnostic loop-back mode
- Fully synthesizable
- Scan test ready

Deliverables:

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL testbenches
- Reference technology netlist
- Product Specification & User Guide

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Modes of Operation

The M16x50 has 16550A and 16C450 modes, corresponding to operation with and without FIFOs. After a hardware reset, the M16x50 is placed in 16C450 mode. It can then have its FIFOs enabled and enter 16550A mode. The M16x50 then adds further functionality beyond 16550A mode. Each of the extended functions can be selected individually under software control.

Flow Control

The M16x50 offers both hardware flow control (in which the transmission and reception of data characters is controlled via the RTS and CTS modem status signals) and software flow control (in which transmission and reception are controlled via the transmission of 'XON/XOFF' characters).

Hardware transmission and reception flow control can be enabled separately. When hardware transmission flow control is enabled, the M16x50 disables transmission when the CTS modem control signal is sampled inactive. When hardware reception flow control is enabled, the M16x50 forces the RTS signal to its inactive state when the Receive FIFO exceeds a pre-set trigger level.

Software reception flow control works by comparing received data characters with the XOFF character. Software transmission flow control works by sending the XOFF character when the Receive FIFO exceeds its threshold level. As soon as the Receive FIFO has fallen below its threshold level, the XON character is transmitted to re-enable transmission from the other end of the link.

On reset, the characters in the XON/XOFF registers are defined by configuration constants. The normal default is to reset them to 00h: this ensures compatibility with existing driver software.

IRDA Modulation/Demodulation

Basic IrDA 1.0 SIR modulation/demodulation has been added to the M16x50 UART. This feature uses the x16 TXCLK and RXCLK to generate $^{3}/_{16}$ width pulses.

Character Timeout

Two signals – CR and TOT – have been added to the M16x50 in order to support system implementations that use an external timer to detect an end of data packet when no characters have been received for a time-out period. CR is always active, whereas TOT is only active when software flow control is enabled.

Reference Technology Gate Count: 9500 (with 16 byte FIFO)

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Signal Description

The M16x50 has 44 external signals; 23 inputs and 21 outputs.

CPU INTERFACE SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
CLOCK	Input	Master clock input.
RESETN	Input	Master reset (active low). De-asserts VAL and ACK.
ADDRESS [2:0]	Input	Address lines.
RD	Input	Read/Write indicator The register read/written is defined by ADDRESS[2:0] & DLAB (LCR[7]).
VAL	Input	CPU Access Validate.
ACK	Output	COU Access Acknowledge.
WDATA [7:0]	Input	Data bus input. Must be valid during write cycles.
RDATA [7:0]	Output	Data bus output. Register returned depends on the state of ADDRESS[2:0] & DLAB (LCR[7]).
NDVL	Output	Data bus output valid (active low). Can be used to control a bi-direct buffer for the data bus.
IRQ	Output	Interrupt request (active high). Goes high whenever one of the enabled interrupts becomes valid.
RXRDY	Output	DMA handshake. Goes low when the RX FIFO contains data.
TXRDY	Output	DMA handshake. Goes low when the TX FIFO requires data.
SERIAL INTERFACE SIGNALS		
BAUD	Output	Baud Rate Generator output clock. When the baud rate generator divisor is 1, this signal is permanently high. For divisors greater than 1, this signal has an output frequency equal to the input frequency of CLK divided by the baud rate generator divisor.
RCLK	Input	External Receive Clock input.
RCLK_ BAUD	Input	Receive Clock Select. When high, the receiver is clocked from the output of the baud rate generator. When low, the receiver is clocked from the RCLK input.
BRGE	Input	Baud Rate Generator Enable (active high). When low, the baud rate generator is held in its current state. This signal can be used to add a pre-scaler to the baud rate generator.
SIN	Input	Serial input. Data is clocked in using the baud rate generator (or RCLK), divided by 16.
SOUT	Output	Serial output. Data is clocked out using the baud rate generator, divided by 16.
NDCD	Input	Data Carrier Detect, MSR[7] status bit (active low).
NRI	Input	Ring Indicator, MSR[6] status bit (active low).
NDSR	Input	Data Set Ready, MSR[5] status bit (active low)
NCTS	Input	Clear To Send, MSR[4] status bit (active low). Also used for hardware flow control.
NOUT1	Output	General control, MCR[2] control bit (active low).
NOUT2	Output	General control, MCR[3] control bit (active low).
NRTS	Output	Request To Send, MCR[1] control bit (active low). Also used for hardware flow control.
NDTR	Output	Data Terminal Ready, MCR[0] control bit (active low).
CR	Output	Character Received. Goes high for 1 Receive clock when a character is received.
TOT	Output	Transmitter Off Transmitted. Goes high after an XOFF character is transmitted.

Note: The address latch included in the original device is not included in the M16x50 in order to allow the design to be scan testable. This latch can be implemented externally if required.

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04/05 PD-4011099.003-FO