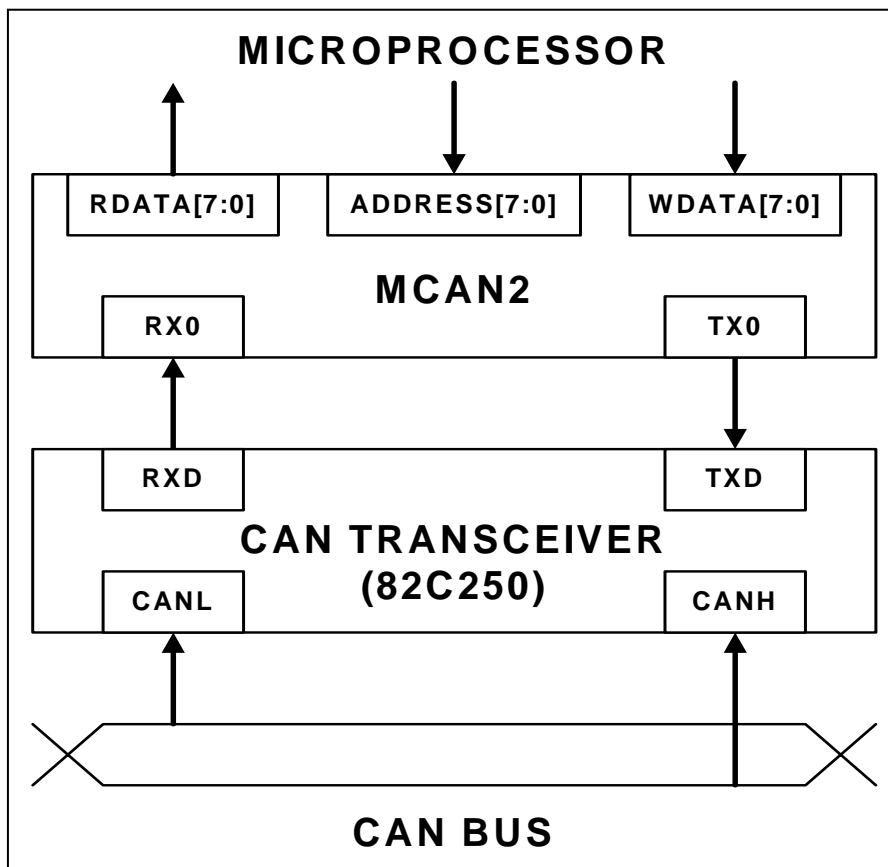


Inventra™ MCAN2

CAN 2.0 Network Controller

Soft Core (RTL IP)

D A T A S H E E T



MCAN2 Block Diagram

Overview

The Inventra™ MCAN2 is a stand-alone controller for a Controller Area Network. It provides an interface between a microprocessor and a CAN bus which carries out all the actions of data encoding/decoding, message management, bit timing and re-synchronization involved in transmitting and receiving data over a CAN network.

The MCAN2 implements the BOSCH CAN Message Transfer Protocols 2.0A and 2.0B. Specification 2.0A is equivalent to CAN 1.2 and covers standard message formats (11-bit identifiers); specification 2.0B covers both standard and extended message formats (both 11-bit and 29-bit identifiers).

The MCAN2 is broadly compatible with a Philips SJA1000 working in its PeliCAN mode. Its CPU interface is compatible with the Peripheral Virtual Component Interface (defined by VSIA) for ease of connection to a range of microprocessor buses.

Major Product Features:

- Supports full CAN 2.0 – both 2.0A (equivalent to CAN 1.2) and 2.0B
- Supports 11-bit & 29-bit identifiers
- Supports bit rates from less than 125KBaud to more than 1MBaud
- 64-byte Receive FIFO
- Synchronous PVICI* -compatible CPU interface for easy connection to a range of microprocessors
- Acceptance filtering
- Software-driven bit-rate detection allowing hot plug-in support
- Listen-Only & Self-Reception modes
- Self Test option
- Interrupt generated for each bus error
- Arbitration lost interrupt with record of bit position
- Read/write error counters
- Programmable error limit warning
- Broadly compatible with Philips SJA1000 in its PeliCAN mode
- Fully synthesizable
- Verified against Bosch CAN2.0 test suite

Deliverables:

- Verilog and VHDL source code
- Synthesis script for Design Compiler
- Verilog and VHDL testbench
- Reference technology netlist
- Product Specification, User Guide & Programmer's Guide

* Peripheral Virtual Component Interface, as defined by VSIA (OCB 2 v1.0)

Functional Description

The CPU accesses the MCAN2 controller through separate address, input data and output data buses.

Messages for transmission are placed in the Transmit Buffer from where they are transmitted by the Transmit Engine within the Bit Processor. Messages received are first filtered by an Acceptance Filter, then placed in the Receive FIFO.

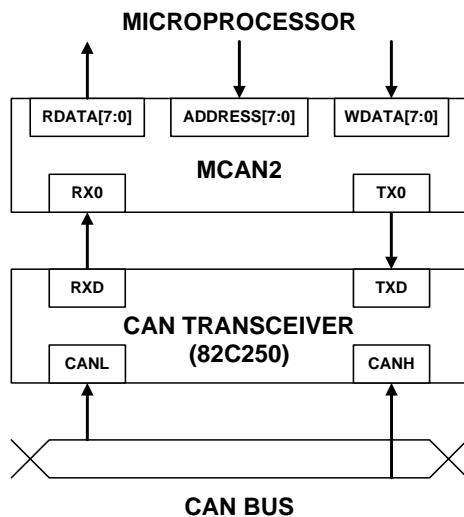
The CPU accesses the Receive FIFO through a 13-byte window referred to as the Receive Buffer. The use of the Receive Buffer in conjunction with the Receive FIFO allows the CPU to process one message while other messages are being received. The Receive FIFO is 64 bytes in length and is used in circular fashion, giving it the capacity to accommodate up to five Extended Frame Format messages at a time.

The interface to the CAN bus is provided by the TX0, TX1 and RX0 signals. TX1 is normally the inverse of TX0 but can be programmed to output the Transmit clock if required.

Intended Use

The MCAN2 is designed to sit between a Host microprocessor and a standard CAN bus transceiver. The transceiver is responsible for putting logical levels from the MCAN2 onto the CAN bus. The CAN bus itself is usually a twisted pair which is fed into the differential inputs of the CAN transceiver.

The figure below shows the usual arrangement in which TX0 drives the CAN transceiver. However, the TX1 output (described above) gives the system designer the option of creating their own interface to the CAN bus instead of using a standard CAN transceiver.



Signal Description

The MCAN2 has 40 external signals; 24 inputs and 16 outputs.

SYMBOL	TYPE	DESCRIPTION
WDATA[7:0]	Input	Data bus input.
ADDRESS[7:0]	Input	Address bus.
XTAL1	Input	System clock.
RX0	Input	CAN bus input (from CAN transceiver).
NRST	Input	Reset, active low.
VAL	Input	CPU Access Validate.
RD	Input	CPU Read signal.
NINT_IN	Input	Input from NINT bi-direct buffer. Used to wake device from Sleep Mode.
TEST	Input	Test pin (to allow better fault coverage).
RDATA[7:0]	Output	Data bus output.
CLKOUT	Output	Clock output signal derived from divided input clock.
NINT	Output	Interrupt output. Used to interrupt the host microcontroller.
NINT_EN	Output	Enable for Interrupt signal, which is open-drain.
TX0	Output	Serial output for CAN output driver 0.
TX1	Output	Serial output for CAN output driver 1.
TX0_EN	Output	Enable signal for TX0.
TX1_EN	Output	Enable signal for TX1.
XTAL1_IN	Input	Gated system clock.
NXTAL1_ENABLE	Output	Enable for XTAL1_IN, active low. Used to disable XTAL1_IN while in Sleep Mode.

Acceptance Filtering

The MCAN2 allows pre-filtering of received messages by applying an Acceptance Filter to received data. Only the messages with identifier bits that match the filter are passed to the Receive FIFO.

The filtering is carried out using four 8-bit Acceptance Code Registers (which record the bit patterns to match), together with four 8-bit Acceptance Mask Registers which mark particular bits of the Acceptance Code bit patterns as 'don't care'. Both sets of registers are applied either as a single 32-bit filter to the first 4 bytes of each received message, or as two separate 16-bit filters to the first 2 bytes of the message.

The Acceptance Mask Registers allow groups of messages with similar identifiers to be accepted.

Reference Technology Gate Count: 22000

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