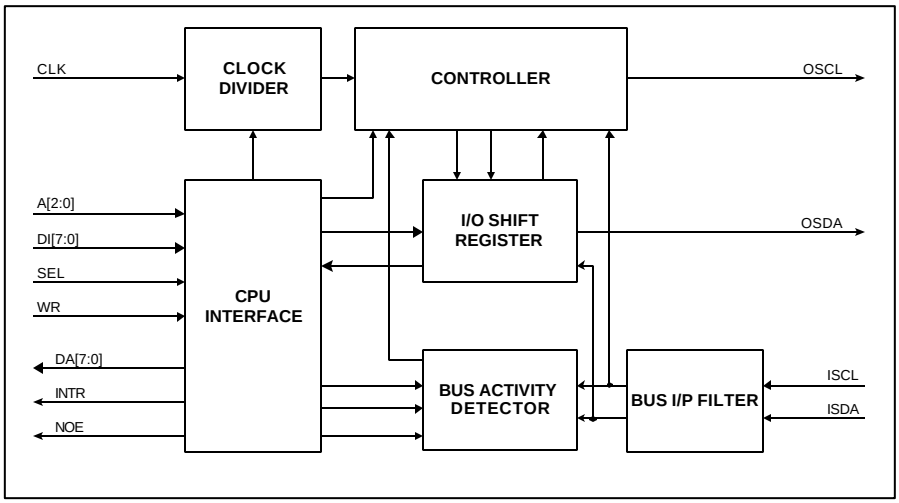
Inventra™ MI2C
I²C bus interface

Soft Core (RTL IP)

D A T A S H E E T



MI2C Block Diagram

Overview

The MI2C provides an interface between a microprocessor and an I²C bus. It can be programmed to operate as either a master or a slave device and performs arbitration in master mode to allow it to operate in multi-master systems.

In slave mode, it can interrupt the processor when it recognizes its own 7-bit or 10-bit address or the general call address.

The MI2C can be used in any applications which use I²C bus devices. These are primarily in the consumer and telecoms market segments. The I²C bus is also used as a board level communications protocol.

Major Product Features:

- Master or slave operation
- Multi-master systems supported
- Allows 10-bit addressing with I²C bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies
- Synchronous processor interface
- Fully synthesizable

Deliverables:

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL testbenches
- Reference technology netlist
- Product Specification & User Guide

Related Products:

- MI2CV I²C V1 Bus Interface with PVCI-compatible CPU interface
- MI2Cv2 I²C V2 Bus Interface

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Operating Modes

The MI2C can operate in four modes: Master Transmit; Master Receive; Slave Transmit; and Slave Receive.

The MI2C will automatically enter Slave Transmit mode if it receives its own Slave Address and a Read bit.

It will similarly enter Slave Receive mode if it receives either its own Slave Address and a Write bit, or the General Call Address.

Status Information

The state of the interface at any time is indicated by the status code recorded in the MI2C's STAT register.

There are 28 status codes corresponding to the different possible states of the MI2C, plus a further code that indicates when no relevant status information is available. The states reported cover all conditions from successful transmission to bus errors and loss of arbitration.

The appropriate microprocessor responses to the reported interface condition and the MI2C actions these invoke are detailed in the MI2C Product Specification.

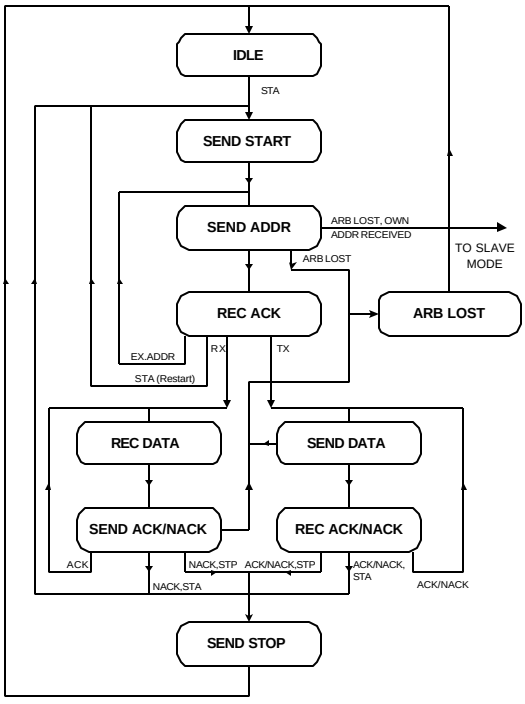
Signal Description

The MI2C has 29 external signals; 17 inputs and 12 outputs.

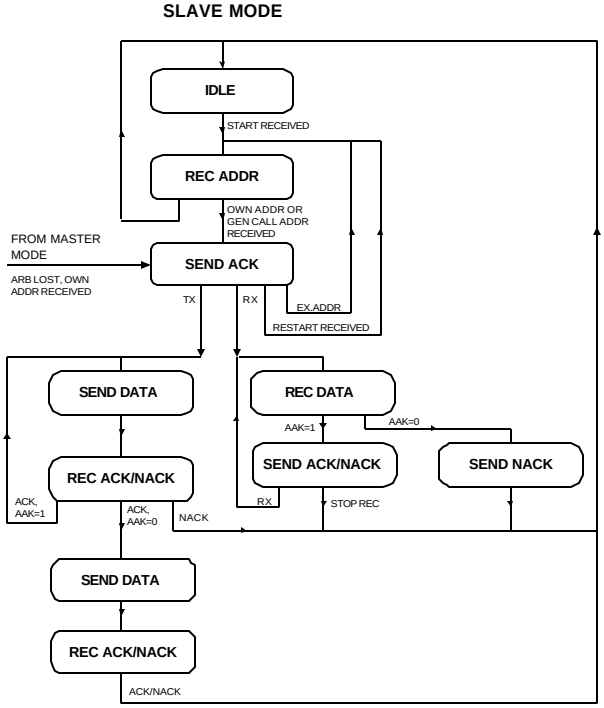
SIGNAL	TYPE	DESCRIPTION
ISDA	Input	I²C bus data line (input)
ISCL	Input	I²C bus clock line (input)
DI[7:0]	Input	Processor data bus (input)
A[2:0]	Input	Processor address lines
SEL	Input	Processor select line
WR	Input	Processor write enable
NRST	Input	Reset, active low
CLK	Input	Clock
NOE	Output	Data bus output enable, active low
DA[7:0]	Output	Processor data bus (output)
INTR	Output	Processor interrupt line
OSDA	Output	I²C bus data line (output)
OSCL	Output	I²C bus clock line (output)

Reference Technology Gate Count: 2000

MASTER MODE



SLAVE MODE



Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, OR 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

European Headquarters
Mentor Graphics Corporation
Immeuble le Pasteur
13/15, rue Jeanne Braconnier
92360 Meudon La Foret
France
Phone: 33-1-40-94-74-74
Fax: 33-1-46-01-91-73

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F,
International Trade Building
No.333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-2756027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

02/02 PD-40026.005-FO