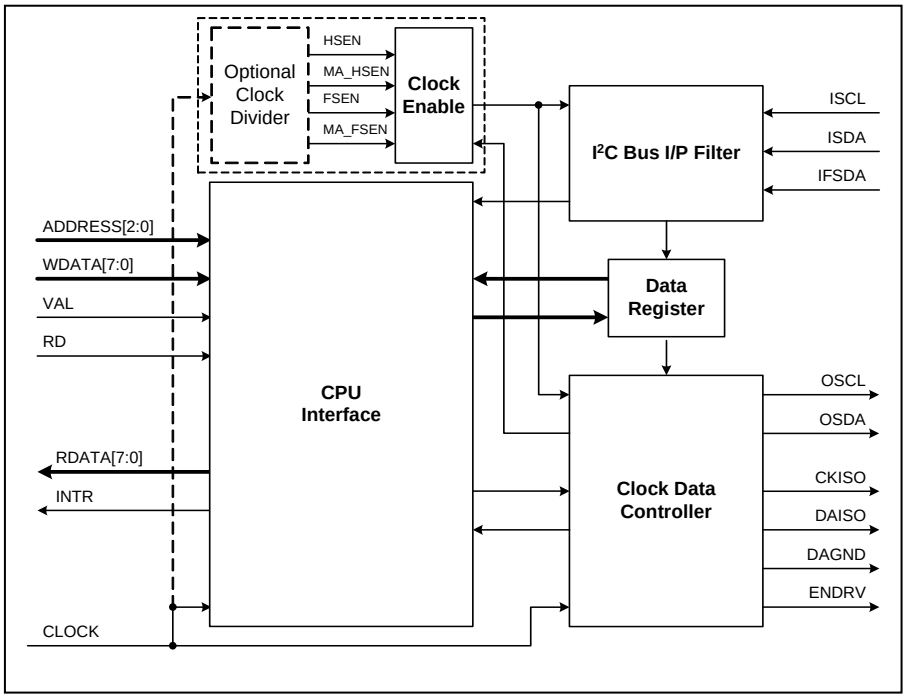
MI2Cv2
I²C V2 Bus Interface

Soft Core (RTL IP)

D A T A S H E E T



MI2Cv2 Block Diagram

Overview

The MI2Cv2 provides an interface between a microprocessor and an I²C bus that conforms to V2.1 of the I²C bus specification.

It can be programmed to operate as either a master or a slave device and performs arbitration in master mode to allow it to operate in multi-master systems. In slave mode, it can interrupt the processor when it recognizes its own 7-bit or 10-bit address or the general call address.

The design supports both High speed (Hs) and Fast / Standard speed (F/S) transfer rates. The user may define the transfer rate using either two clock enable signals or a pair of clock control registers similar to that offered in the Inventra™ MI2C and MI2CV designs.

Access to the core's internal control and status registers is provided via a synchronous PVCI*-compatible CPU interface (with default acknowledge). This interface allows the core to be readily interfaced to a range of popular on-chip buses such as the AMBA bus and the buses associated with the IBM CoreConnect™ architecture.

The MI2Cv2 can be used in any application that uses I²C bus devices. These are primarily in the consumer and telecommunications market segments. The I²C bus is also used as a board-level communications protocol.

Major Product Features:

- Conforms to V2.1 of the I²C bus specification
- Supports High speed (3400kbits/s), Fast and Standard transfer rates
- Supports bus isolation
- Master or slave operation
- Multi-master systems supported
- Supports both 7-bit and 10-bit addressing on the I²C bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Allows operation from a wide range of input clock frequencies
- 8-bit PVCI*-compatible synchronous CPU interface
- Fully synthesizable

Deliverables:

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL testbenches
- Reference technology netlist
- Product Specification & User Guide

Related Products:

- MI2CV V1 I²C Bus Interface with PVCI-compatible CPU Interface

* Peripheral Virtual Component Interface, as defined by VSIA (OCB 2 v2.0)

Operating Modes

The MI2Cv2 can operate in four modes: Master Transmit; Master Receive; Slave Transmit; and Slave Receive. The MI2Cv2 will automatically enter Slave Transmit mode if it receives its own Slave Address and a Read bit. It will similarly enter Slave Receive mode if it receives either its own Slave Address and a Write bit, or the General Call Address.

Status Information

The state of the interface at any time is indicated by a status code in the MI2Cv2's STAT register. There are 29 status codes corresponding to the different possible states of the MI2Cv2, plus a further code that indicates when no relevant status information is available. The states reported cover all conditions from successful transmission to bus errors and loss of arbitration. The way the microprocessor should respond to the different conditions is detailed in the MI2Cv2 Product Specification.

Signal Description

The MI2Cv2 has 37 external signals; 22 inputs and 15 outputs.

SIGNAL	TYPE	DESCRIPTION
CLOCK	Input	Master Clock Input
HSEN	Input	Sample Clock Enable, High speed (Hs) mode
MA_HSEN	Input	Data Rate Clock Enable, High speed (Hs) mode
FSEN	Input	Sample Clock Enable, Fast/Standard speed (F/S) mode
MA_FSEN	Input	Data Rate Clock Enable, Fast/Standard speed (F/S) mode
ADDRESS[2:0]	Input	Processor address lines
WDATA[7:0]	Input	Processor input data bus
VAL	Input	CPU Access Validate
RD	Input	Read/Write Indicator
ISCL	Input	I²C bus input clock line
ISDA	Input	Hs I²C bus input data line
IFSDA	Input	F/S I²C bus input data line
RESETN	Input	Master Reset, active low
RDATA[7:0]	Output	Processor output data bus
CKISO	Output	Isolate F/S SCL
DAISO	Output	Isolate F/S SDA
DAGND	Output	Drive F/S SDA to ground
INTR	Output	Processor interrupt line
ENDRV	Output	Enables active pull-up of SCL during Hs data transfer
OSCL	Output	I²C bus output clock line
OSDA	Output	I²C bus output data line

Reference Technology Gate Count: 1800

Bus Clock Speed

The rate at which data is transmitted or sampled from the I²C bus is defined by four clock enables, two for Fast/Standard mode (FSEN and MA_FSEN) and two for High speed mode (HSEN and MA_HSEN). The I²C bus is defined for bus clock speeds up to 100 kbits/s in 'Standard mode', 400 kbits/s in 'Fast mode' or 3400 kbits/s in 'High speed mode' and the sampling rate must be at least10x the maximum data rate in the specified mode.

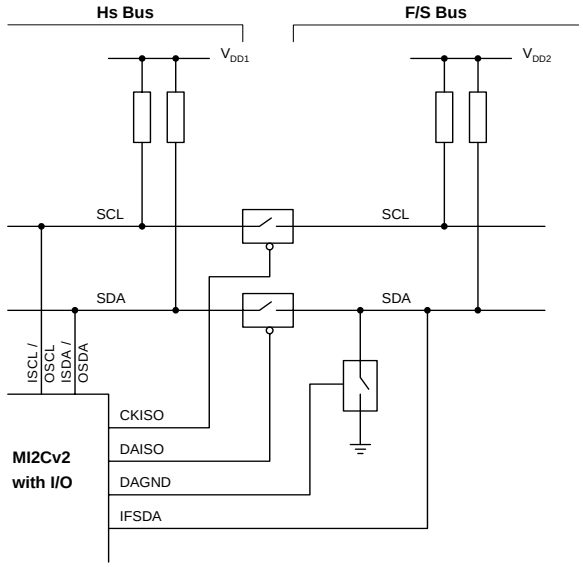
The required FSEN, MA_FSEN, HSEN and MA_HSEN signals can either be generated externally or by the clock divider that may optionally be included in the MI2Cv2 design.

High Speed Mode

A Master may arbitrate and select high speed operation by transmitting one of the reserved 7-bit addresses of the form 00001*xxx*b. The first five bits of this address are significant: the remaining three bits may be used to identify different High speed mode masters on the same I²C bus. On detecting a code of this form, the MI2Cv2 enters High speed mode. It will revert to Fast/Standard speed mode on detection of a STOP condition on the I²C bus.

Bus Isolation

I²C devices that only operate at Fast/Standard (F/S) speed may be confused by High speed (Hs) data. To prevent this, the MI2Cv2 has additional control logic which isolates the F/S portion of the I²C bus from the high speed section during high speed data transfers and a separate F/S I²C bus data input line IFSDA.The diagram below shows how the signals involved – CKISO, DAISO and DAGND – and the IFSDA data input line might be connected.



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