MICROCONTROLLER/PROCESSOR

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THE INTELLIGENT APPROACH TO INTELLECTUAL PROPERTY

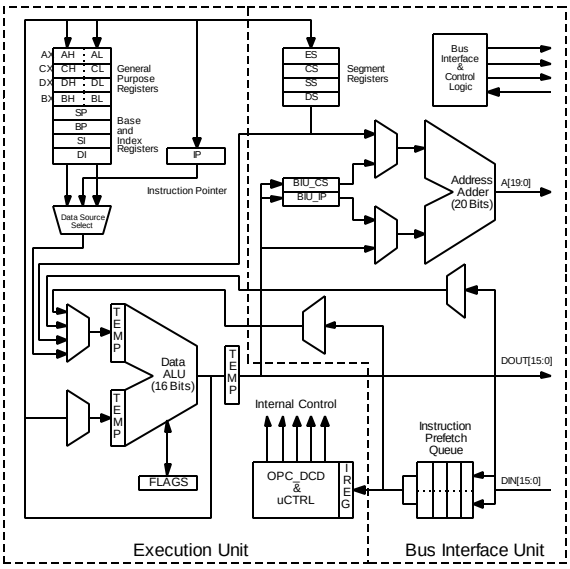
M8086

16-BIT MICROPROCESSOR

OVERVIEW

The M8086 implements the industry standard 8086 microprocessor, but also includes additional 80186 instructions. This feature allows the M8086 to be fully software compatible with the Intel 8086, 8088, 80186, and 80188 family of processors, while offering improved Bus Interface Timings, faster Instruction Execution and Address calculation times. Other features include an increase in the Instruction Pre-Fetch Queue to 8 Bytes, Maskable/Non-Maskable Interrupt capability and the choice of a 8 or 16-bit external data bus.

BLOCK DIAGRAM



KEY FEATURES

- Instruction Execution improved by 50% in some cases
- Instruction Pre-Fetch Queue increased to 8 Bytes
- Improved Bus Interface Timing
- 3 Clock or 4 Clock bus interface
- Powerful Addressing Modes
- Effective address calculation times reduced to 1-4 clocks
- Maskable and Non-Maskable Interrupt Capability
- 80186 Instructions included
- Fully synthesizable

DELIVERABLES

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL test benches

SOFT CORES

DESIGN OVERVIEW

The M8086 comprises two major functional blocks - an Execution Unit (EU) and a Bus Interface Unit (BIU) - which operate independently and asynchronously to each other.

The EU has no external connection and receives instructions from a queue maintained by the BIU. Where an instruction requires access to memory or a peripheral device, the EU requests the BIU to obtain or store the data.

The BIU performs all bus operations for the EU with data being transferred between the M8086 and memory / I/O upon demand from the BIU. During periods when the EU is busy executing instructions, the BIU looks "ahead" and fetches more instructions from memory which it stores in a pre-fetch queue.

SPECIAL FEATURES

ENHANCED INSTRUCTION TIMING: The M8086 has been designed to execute instructions in fewer clocks than in the standard devices.

In addition, the external bus cycle timing has been compressed to 3 clocks, though a 4 clock bus cycle may be used if required.

Together these offer an increase of up to 50% in the instruction throughput for a given instruction sequence.

INSTRUCTION PRE-FETCH QUEUE: The M8086 provides up to 8 Bytes for the Instruction Pre-Fetch Queue when used with a 16-bit external bus. This compares with a maximum of 6 Bytes in the industry standard 8086. (When configured for an 8-bit external bus, the queue can be up to 4 Bytes.)

80186 INSTRUCTION SET: The following 80186 instructions have been included in the M8086: PUSH immediate; PUSHA; POP immediate; POPA; IMUL; SHR Register by Count; SHR Memory by Count; INS; OUTS; ENTER; LEAVE; and BOUND.

SYNTHESIS OPTIONS

BUS CYCLE: Opting to synthesize the M8086 in its enhanced 3-clock mode gives the device a 3-clock external bus cycle, but an industry standard 8086 compatible mode may be selected instead if a 4-clock external bus cycle is required.

ESC OPCODE ACTION: The M8086 can be set either to perform a memory cycle like a 8086 or to generate an ESC opcode exception like a 80186.

SIGNAL DESCRIPTION

The M8086 has 90 external signals: 23 inputs and 67 outputs.

PROCESSOR INPUT SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
CLK	Input	External Clock Input
DIN[15:0]	Input	The input section of the 16-bit data bus
RES_N	Input	Reset
SRDY	Input	Synchronous Ready
TEST_N	Input	Test input
HOLD	Input	Hold Request - used when another bus master is requesting use of the bus
NMI	Input	Non-Maskable Interrupt
INTR	Input	Interrupt Request

PROCESSOR OUTPUT SIGNALS		
ADLOE,ADHOE	Output	Address/Data Bus Output Enables
ADDR[23:0]	Output	Address Bus: able to address up to 16MB of physical memory
DOUT[15:0]	Output	Data Bus Out
MXADS	Output	Multiplexed Address/Data Bus Select
BHE_N	Output	Byte High Enable
ALE	Output	Address Latch Enable
RD_N	Output	Read (active low)
WR_N	Output	Write (active low)
INTA_N	Output	Interrupt Acknowledge
DTR_N	Output	Data Transmit/Receive
DEN_N	Output	Data Enable
LOCK_N	Output	Lock Bus
RESET	Output	Synchronized Reset
STATUS[7:0]	Output	Status Bus
SDIS	Output	Status Disable
QS[1:0]	Output	Queue Status
HDLA	Output	Hold Acknowledge
CSOE	Output	Control Signals Output Enable
SOE	Output	Status Output Enable
DENOE	Output	Data Enable Output Enable

EXTERNAL DATA BUS SIZE: The internal M8086 execution unit is always 16-bit but the external data bus may be 16-bit or 8-bit.

The supplied test bench is automatically configured to reflect the selections made.

REFERENCE TECHNOLOGY GATE COUNT: 18000

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