MICROCONTROLLER/PROCESSOR

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THE INTELLIGENT APPROACH TO INTELLECTUAL PROPERTY

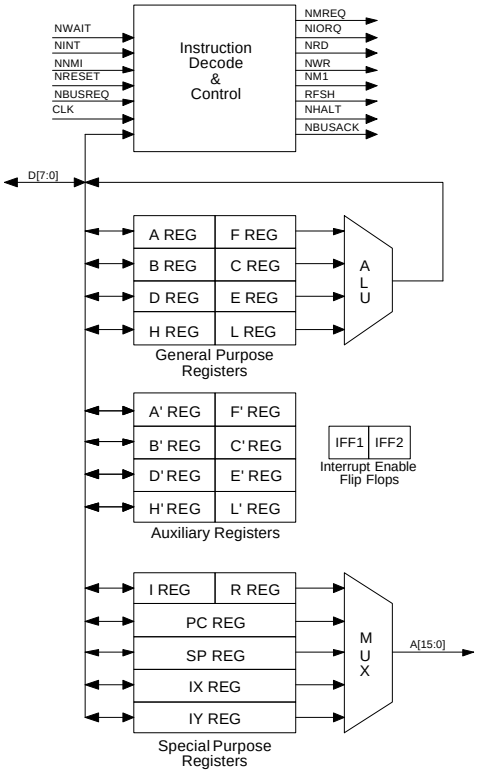
MZ80

8-BIT MICROPROCESSOR

OVERVIEW

The MZ80 is a high performance 8-bit microprocessor which is software compatible with the Zilog Z80 family. It has a powerful instruction set which includes block transfers, bit test, set, and reset instructions. Fast context switches are supported via an auxiliary register set.

BLOCK DIAGRAM



KEY FEATURES

- 158 Instruction Types
- 10 Addressing Modes
- 8-bit ALU with Binary and Decimal Arithmetic Instructions
- 64Kbyte Address space
- Block Transfer and Search Instructions
- Bit Test, Set, and Reset Instructions
- Alternate Register Set
- Non-Maskable/Maskable Interrupt Capability
- Fully synthesizable
- Silicon verified

DELIVERABLES

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL test benches
- Reference technology netlist

SOFT CORES

FUNCTIONAL DESCRIPTION

The Instruction Decode and Control block is responsible for the operation of the MZ80, and outputs all the control signals for the registers, ALU, data path and address select multiplexers.
The ALU performs arithmetic and logical instructions from data contained in eight General Purpose 8-bit Registers. Displacement calculations for the index registers and the program counter are also computed by the ALU.

The Auxiliary Register file contains four register pairs. These registers allow for fast context switching by exchanging the contents of each register file back and forth.

Six Special Purpose Registers are included. These offer a powerful method of indexing data stored in memory.

INSTRUCTION SET

One of the features of the Z80 processor is its rich instruction set.

In addition to load instructions, I/O instructions, general arithmetic instructions, logic instructions, jumps, calls, rotates and shifts, the MZ80 also offers bit operations, block transfers, block searches, plus the facility to make an alternative set of registers accessible to the programmer. This last option makes it easy to switch between background and foreground tasks.

The MZ80 product specification lists all 158 instruction types, together with details of the flags set, the number of machine cycles taken by each instruction and the number of T-states generated.

INTERRUPT SYSTEM

The MZ80 accepts two interrupt input signals, NNMI and NINT. NNMI is a non-maskable interrupt and has the highest priority. NINT is a lower priority interrupt which only operates if interrupts are enabled in software.

The MZ80 has a single response mode for servicing the non-maskable interrupt, but offers a choice of three programmable response modes for maskable interrupts:

Mode 0 - 8080 compatible
Mode 1 - Peripheral Interrupt service
Mode 2 - A vectored interrupt scheme for Z80 family with or without daisy chain

The MZ80 services interrupts by sampling the NNMI and NINT signals on the last clock of an instruction.

SIGNAL DESCRIPTION

The MZ80 has 49 external signals: 15 inputs and 34 outputs.

MZ80 INPUT SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
CLK	Input	External Clock input
NCLK	Input	Inversion of Clock Input
DIN[7:0]	Input	Data Bus In
NWAIT	Input	Used to insert wait states during bus cycles
NINT	Input	Level sensitive maskable interrupt request signal
NRESET	Input	Reset
NBUSREQ	Input	Bus Request
NNMI	Input	Non-Maskable Interrupt

MZ80 OUTPUT SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
NAOE	Output	Address Output Enable
ADDR[15:0]	Output	Address Bus
DOUT[7:0]	Output	Data Bus Out
NDOE	Output	Data Out Enable
NMREQ	Output	Memory Request
NIORQ	Output	I/O Request
NRD	Output	Read (active low)
NWR	Output	Write (active low)
NCOE	Output	Control Output Enable
NM1	Output	Machine Cycle 1
NHALT	Output	Indicates MZ80 has executed a halt instruction
NBUSACK	Output	Bus Acknowledge

ADDRESSING MODES

The MZ80 has twelve addressing modes: Immediate; Immediate Extended; Modified Page Zero; Relative; Extended; Indexed; Register; Implied; Register Indirect; Register Bit; Register Indirect Bit; and Indexed Bit.

It also offers a Mixed Addressing mode in which more than one of the above modes are used in conjunction with each other.

REFERENCE TECHNOLOGY GATE COUNT: 8000

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, OR 97070-7777
U.S.A.
Phone: 503-685-7000
Fax: 503-685-1202

General Information
Mentor Graphics Corporation
P.O. Box 5050
Wilsonville, OR 97070-5050
U.S.A.
Phone: 800-547-3000
Phone: 503-685-8000
Fax: 503-685-8001

European Headquarters
Mentor Graphics Corporation
Immeuble le Pasteur
13/15, rue Jeanne Braconnier
92360 Meudon La Foret
France
Phone: 33-1-40-94-74-74
Fax: 33-1-46-01-91-73

Pacific Rim Headquarters
Mentor Graphics Singapore PTE Ltd.
51 Science Park Drive
The Faraday
Singapore Science Park
Singapore 118231
Phone: 65-779-0075
Fax: 65-870-2799

Japanese Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

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