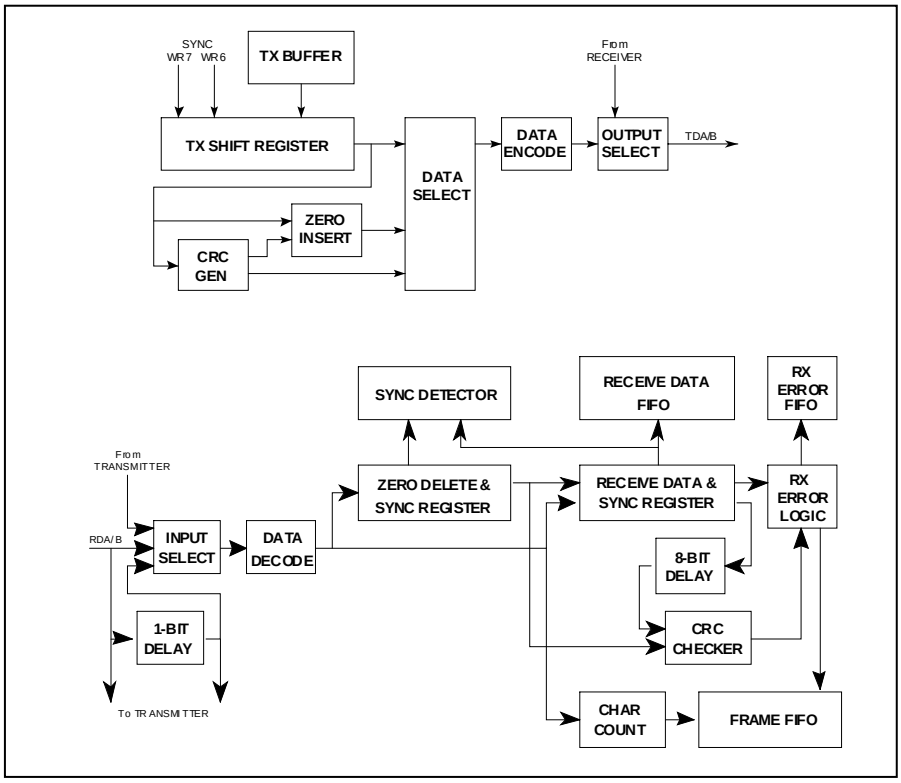
M85230: Enhanced version of M85C30 Serial Communications Controller

Soft Core (RTL IP)

D A T A S H E E T



M85230 Transmitter and Receiver Blocks

Overview

The M85230 is an enhanced version of the Mentor Graphics M85C30 serial communications controller. The enhancements include: a deeper Transmit FIFO (4bytes); a deeper Receive FIFO (8 bytes); a programmable FIFO level for interrupts and DMA requests; latching of Read registers during reads; and automatic forcing of TxD pin high in Mark Idle mode.

The M85230 has two independent full-duplex channels which support asynchronous, bit synchronous (SDLC, HDLC and SDLC loop mode) and byte synchronous (MONOSYNC*, BISYNC*) communication modes.
NRZ, NRZI and FM data encoding/decoding are supported.

It is fully programmable through its 8-bit system interface.

Two diagnostic modes – local loop-back and automatic echo – are offered.

* Please note that the support for these modes is not as fully tested as that for the other, more commonly required modes.

Major Product Features:

- Software compatible with the Zilog Z85230
- Supports both asynchronous and synchronous communication modes
- SDLC loop-mode supported
- NRZ, NRZI and FM encoding/decoding
- 4byte Transmit FIFO; 8 byte Receive FIFO
- Two independent full-duplex channels
- Digital phase-locked loop for each channel
- Baud rate generator for each channel
- Local loop-back and automatic echo modes
- Character counter and 10x19-bit frame status FIFO in SDLC mode
- Fully synthesisable

Deliverables:

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL testbenches
- Reference technology netlist
- Product Specification & User Guide

Related Product:

- M85C30 Serial Communications Controller with FIFOs

Structure

Each of the two identical channels in the M85230 contain a transmitter, a receiver, a baud rate generator, a digital phase-locked loop and a clock selector that provides the clocks for the transmitter and the receiver blocks.

The clocks can be programmed to come from one of two external clocks, from the baud rate generator, or they can be derived from the receiver data stream by the phase-locked loop.

In addition to the two serial communication channels, there is a common 8-bit system interface and a six-source interrupt controller.

Special Features of the M85230

In addition to the facilities provided by the M85C30, the M85230 also provides:

- A 4-byte Transmit FIFO (c.f. a single character Write Buffer)
- An 8-byte Receive FIFO (c.f. a single character Read Buffer)
- Programmable FIFO trigger levels
- Read register latching
- Automatic forcing of TxD pin high in Mark Idle mode

Data Encoding/Decoding

The M85230 provides four data encoding methods: Non-Return to Zero (NRZ); Non-Return to Zero Inverted (NRZI); Biphase Mark (FM1); Biphase Space (FM0). The M85230 can also be used to decode Manchester encoded data.

All the encoding methods can be used in all operating modes except SDLC Loop mode, in which only NRZ or NRZI can be used. In FM mode, the M85230 can transmit and receive with either 1x, 16x or 32x Clock Mode selected.

The data encoding is active even when the transmitter or receiver is idling or disabled.

Signal Description

The M85230 has 62 external signals; 31 inputs and 31 outputs.

SIGNAL	TYPE	DESCRIPTION
CLK	Input	System Clock
NCLK	Input	Inverse of System Clock
DI[7:0]	Input	Input data bus
DA[7:0]	Output	Output data bus
NDOE	Output	Data bus direction control (low = output)
DNC	Input	Data/command select (high = data)
ANB	Input	A/B channel select (high = channel A)
NCS	Input	Chip select (active low)
NWR	Input	Write strobe (active low)
NRD	Input	Read strobe (active low)
NINTA	Input	Interrupt acknowledge (active low)
NINT	Output	Interrupt request (active low)
IEI	Input	Interrupt enable in
IEO	Output	Interrupt enable out
NRDQA	Output	Wait/Request chan.A (active low)
NRDQB	Output	Wait/Request chan.B (active low)
WNRAE	Output	Wait/Request mode enable, chan.A
WNRBE	Output	Wait/Request mode enable, chan.B
NRST	Input	Reset (active low)
NSYAI	Input	Synchronisation in, chan. A (active low)
NSYAO	Output	Synchronisation out, chan.A (active low)
NSYAE	Output	Sync direction control, chan.A (low = out)
TRCAI	Input	Transmit/receive clock input, chan.A
TRCAO	Output	Transmit/receive clock output, chan.A
NTCAE	Output	Tx/Rx clock direction control, chan.A (low = out)
RTCA	Input	Receive/transmit clock, chan.A
RDA	Input	Receive data, chan.A
TDA	Output	Transmit data, chan.A
NSYBI	Input	Synchronisation in, chan.B (active low)
NSYBO	Output	Synchronisation in, chan.B (active low)
NSYBE	Output	Sync direction control, chan.B (low = out)
TRCBI	Input	Transmit/receive clock input, chan.B
TRCBO	Output	Transmit/receive clock output, chan.B
NTCBE	Output	Tx/Rx clock direction control, chan.B (low = out)
RTCB	Input	Receive/transmit clock, chan.B
RDB	Input	Receive data, chan.B
TDB	Output	Transmit data, chan.B
NDCDA	Input	Carrier detect, chan.A (active low)
NCTSA	Input	Clear to send, chan.A (active low)
NDTRA	Output	Data terminal ready/request, chan.A (active low)
NRTSA	Output	Request to send, chan.A (active low)
NDCDB	Input	Carrier detect, chan.B (active low)
NCTSB	Input	Clear to send, chan.B (active low)
NDTRB	Output	Data terminal ready/request, chan.B (active low)
NRTSB	Output	Request to send, chan.B (active low)
SCAN_TEST _ENABLE	Input	When active (high), disables soft resets to enable scan cell insertion.
TX_CLK_ TEST_A,B	Output	Output clocks used by transmitter A/B. For testbench use only

Reference Technology Gate Count: 17500

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