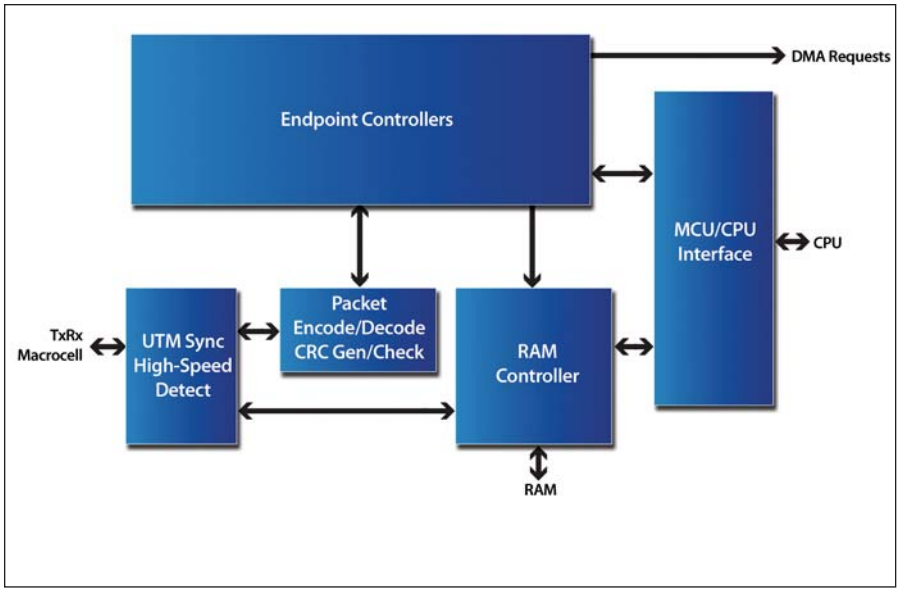
USB 2.0 Core IP

Hi-Speed Function Controller

MUSBHSFC

D A T A S H E E T



MUSBHSFC block diagram.

Hi-/Full-Speed USB Function Controller

The Mentor Graphics® MUSBHSFC core provides a USB function controller that conforms to the USB 2.0 specification for Hi-/Full-Speed (480/12 Mbps) functions.

The core is user-configurable for up to 15 IN Endpoints and up to 15 OUT Endpoints in addition to Endpoint 0 (EP0). These additional Endpoints can be individually programmed for bulk/interrupt or isochronous transfers. Each Endpoint requires an associated FIFO. The MUSBHSFC has a RAM interface for connecting to a single block of synchronous single-port RAM. The FIFO for Endpoint 0 is fixed at 64 bytes. The other Endpoint FIFOs may be from 8 to 192 bytes in size and can buffer either 1 or 2 packets. Separate FIFOs may be associated with each Endpoint. Alternatively, an IN and OUT Endpoint with the same Endpoint number can be configured to use the same FIFO.

The MUSBHSFC provides a USB 2.0 Transceiver Macrocell Interface (UTMI) to connect to an 8/16-bit Hi-/Full-Speed transceiver. Access to the FIFOs and internal control/status registers may be via a 16/32-bit AMBA AHB-compatible synchronous CPU interface via the AMBA AHB bridge. The MUSBHSFC has a RAM interface for connecting to the single block of synchronous RAM that is used for all the Endpoint FIFOs. The device also offers support for DMA access to the Endpoint FIFOs. The device also offers support for DMA access to the Endpoint FIFOs. (The MUSBHSFC-AHB bridge includes DMA controller hooks.)

This Hi-/Full-Speed function controller provides the entire USB packet of encoding, decoding, and checking — interrupting the CPU only when the Endpoint data has been successfully transferred. A graphical user interface script is provided for configuring the core to the user's requirements.

Major product features:

- Complies with USB 2.0 standard for Hi-Speed (480 Mbps) and Full-Speed (12 Mbps)
- Configurable up to 15 additional IN or OUT Endpoints
- Configurable FIFO sizes from 8 to 8,192 bytes with option of dynamic FIFO sizing
- UTMI: USB Transceiver Macrocell Interface
- Built-in 16/32-bit synchronous AMBA AHB-compatible CPU interface
- Support for DMA access to FIFOs
- Synchronous RAM interface for FIFOs
- Supports suspend and resume signaling
- Fully synthesizable
- Scan test ready
- Graphical User Interface provided for core configuration

Deliverables:

- Verilog source code and testbench
- Synthesis script for design compiler

Related products:

- **MUSBMHDRC** - USB OTG Hi-Speed Dual Role Controller
- **MUSBFDRC** - USB OTG Full-Speed Dual Role Controller
- **MUSB-MicroSW** - USB Software Stack
- **MUSBHPHY** - USB Hi-Speed PHY
- **MUSBFPHY** - USB Full-Speed PHY

Signal Description

MUSBHSFC INTERFACE SIGNALS		
UTMI INTERFACE SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
XCLK	Input	Transceiver Macrocell clock. 60MHz/30MHz
XCVRSEL	Output	Transceiver select – Hi-Speed/Full-Speed.
TERMSEL	Output	Termination select – Hi-Speed/Full-Speed.
SUSPENDM	Output	Suspend mode indicator.
LINESTATE[1:0]	Input	Show the current state of D- and D+;
OPMODE[1:0]	Output	Operating mode selector
XDATAOUT[tw:0]	Output	Data to be transmitted, 8- or 16-bit Data Width.
TXVALID	Output	Transmit data valid.
TXVALIDH	Output	High byte of XDATAOUT valid (16-bit bus only).
TXREADY	Input	Transmit data ready.
XDATAIN[tw:0]	Input	Received data. Bus width 8 bits or 16 bits.
RXVALID	Input	Receive data valid.
RXVALIDH	Input	High byte of XDATAIN valid (16-bit bus only).
RXACTIVE	Input	Valid Receive packet indicator.
RXERROR	Input	Receive error indicator.
SOF_PULSE	Output	Frame Sync Pulse.
MCU INTERFACE SIGNALS		
AHB_HSEL	Input	AHB select.
AHB_HREADYI	Input	AHB ready input.
AHB_HREADYO	Output	AHB ready output.
AHB_HSIZE[1:0]	Input	AHB transfer size.
AHB_HTRANS[1:0]	Input	AHB transfer type.
AHB_HADDR[9:0]	Input	AHB address bus.
AHB_HWDATA[31:0]	Input	AHB write data bus.
AHB_HRDATA[31:0]	Output	AHB read data bus.
AHB_HWRITE	Input	AHB write not read
MC_NINT	Output	MCU interrupt. Active low.
Optional DMA INTERFACE SIGNALS		
AHB_HGRANT	Input	AHB bus master grant.
AHB_HRDATAM[31:0]	Input	AHB read data bus (master mode).
AHB_HRESPM[1:0]	Input	AHB response (master mode).
AHB_HBUSREQ	Output	AHB bus master request.
AHB_HTRANSM[1:0]	Output	AHB transfer type (master mode).
AHB_HSIZEM[1:0]	Output	AHB transfer size (master mode).
AHB_HBURSTM[2:0]	Output	AHB burst mode (master mode).
AHB_HWRITEM	Output	AHB write not read (master mode)
AHB_HADDRM[31:0]	Output	AHB address bus (master mode).
AHB_HWDATAM[31:0]	Output	AHB write data bus (master mode).
DMA_NINT	Output	DMA controller interrupt. Active low.
RAM INTERFACE SIGNALS		
RAM_ADDR[rw:0]	Output	RAM Address bus. Variable Width
RAM_DATAI[31:0]	Input	RAM data Input Bus
RAM_DATAO[31:0]	Output	RAM data Output Bus
RAM_NCE	Output	RAM select. Active low.
RAM_NWR	Output	RAM write enable. Active low.
SYSTEM SIGNALS		
CLK	Input	System clock. Must be greater than 30MHz.
NRST	Input	Power-up reset. Active low.
USB_NRSTO	Output	USB function reset Output, Active Low

Structure

The MUSBHSFC function controller consists of a UTM re-synchronizing block, a packet encoder/decoder plus CRC generator/checker block, RAM controller, MCU interface, plus a control block for each Endpoint. The function controller interfaces to a UTMI v1.04 USB 2.0 transceiver macrocell.

USB Transceiver Macrocell (UTM) Sync Block

The role of this block is to resynchronize between the transceiver macrocell (30/60 MHz clock domain) and the function controller's user-supplied clock (>30 MHz). This allows the rest of the MUSBHSFC to run from the bus clock without requiring any further synchronization. If an 8-bit transceiver interface is configured, this block will convert the data to 16-bit so that a user clock down to 30 MHz can be utilized. The block also performs the Hi-Speed detection handshaking.

MCU/CPU Interface

The core may be integrated to a range of different CPU bus standards. The interface provided by the MUSBHSFC is a 16/32-bit synchronous AMBA AHB-compatible CPU interface.

Packet Encoder/Decoder

The packet encoder/decoder block generates headers for packets to be transmitted and decodes the headers of received packets. It also performs CRS generation and checking.

Endpoint Controllers

Utilizes two controller state machines, 1 for control transfers over EP0, and 1 for bulk/interrupt/isochronous transactions EP1-15

RAM Controller

The RAM controller provides an interface to a single block of synchronous RAM, which is used to buffer packets between the MCU and the USB. It takes the FIFO pointers from the Endpoint controllers, converts them to address pointers within the RAM block and generates the RAM access signals.

Reference Technology Gate Count:

- **21,770 [2 Rx & 2 Tx Endpoints + Endpoint 0 (EP0)]**
- **27,188 w/Dynamic FIFO Sizing**

Visit www.mentor.com/ip for additional IP product information.

© 2007 Mentor Graphics Corporation. All Rights Reserved.
Mentor Graphics is a registered trademark of Mentor Graphics Corporation. All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408.436.1500
Fax: 408.436.1501

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: 81.3.5488.3033
Fax: 81.3.5488.3004

Printed on Recycled Paper

MGC - 04/07 1025930-w