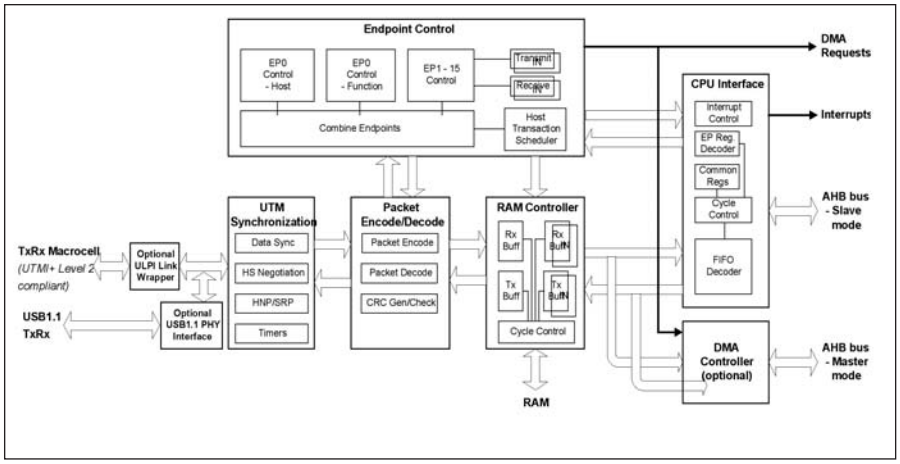
USB 2.0 IP

Multi-Point Hi-Speed OTG Controller

MUSBMHDRC

D A T A S H E E T



The Mentor Graphics multi-point, Hi-Speed dual-role USB controller is supported through the use of an external DMA, or through an internal DMA controller which is built into the AMBA AHB interface.

Multi-Point Hi-Speed OTG Controller

The Mentor Graphics® MUSBMHDRC is a multi-point Hi-Speed dual role USB controller with a complete USB On-The-Go (OTG) capabilities for use in point-to-point communications with other OTG devices and host computers, as well as in multi-point communications with a network of USB 2.0 peripherals and hubs.

The controller complies with both the USB standard for Hi-Speed and Full-Speed functions and the OTG supplement to the USB 2.0 specification.

The approach used in this controller is to allow the core's endpoints to be allocated to the functions of different target devices. Furthermore, this allocation can be made dynamically. In theory, a full USB tree of 128 devices could be supported in this way, though it is likely to be used with much smaller numbers of devices in practice.

The core offers a 32-bit AMBA AHB-compatible CPU interface and a USB 2.0 Transceiver Macrocell Interface (UTMI) + Level 3 transceiver interface together with a wrapper for connecting to a ULPI compatible PHY. (An UTMI+ Level 3 interface is used because it allows the core to support Low-Speed devices attached through a USB 1.1 hub.) An alternative USB 1.1 PHY interface is also provided.

The RAM interface offered by this core is configurable for endpoint FIFO sizes from 8 to 8192 bytes (except for the endpoint 0 FIFO, which is fixed at 64 bytes).

In addition, access to the endpoint FIFOs are supported through the use of an external DMA, or through an internal DMA controller which is built into the AMBA AHB interface.

Point-to-Point Operation

Point-to-point communications are carried out between two USB devices, one operating as a host and the other as a peripheral. In this set-up, the MUSBMHDRC can act either as the host or as the peripheral, and the second device can be either Hi-, Full-, or Low-Speed or another "dual-role" controller.

Major product features:

- Applicable to either point-to-point or multi-point USB OTG
- Complies with the USB 2.0 standard for Hi-Speed (480 Mbps) and Full-Speed (12 Mbps) functions and with the OTG supplement to the USB 2.0 specification
- May be used with High-, Full-, or Low-Speed USB devices
- Can be used as either host or peripheral in point-to-point OTG
- Supports session request protocol (SRP) and host negotiation protocol (HNP)
- Configurable for up to 15 additional transmit endpoints and up to 15 additional receive endpoints
- Configurable FIFOs with option of dynamic FIFO sizing
- 32-bit AMBA AHB-compatible CPU interface supporting multilayer operations
- UTMI+ Level 3 transceiver interface with optional ULPI link wrapper
- Optional USB 1.1 PHY interface
- Synchronous RAM interface for FIFOs
- Support for external DMA access to FIFOs
- Support for internal DMA access to FIFOs via built-in DMA controller
- Performs all transaction scheduling in hardware
- Standard device requests handled efficiently in software for flexibility
- UTMI+ PHY vendor register option
- Graphical user interface provided for core configuration

Deliverables:

- Verilog source code and testbench
- Synthesis script for design compiler
- Reference technology netlist
- Product specification, user guide, and programmer's guide

Signal Description

UTMI+ INTERFACE SIGNALS (LEVEL 3)		
SIGNAL	**TYPE**	**DESCRIPTION**
XCLK	Input	Transceiver macrocell clock. 60MHz(8bit)/30MHz(16bit)
XCVRSEL[1:0]	Output	Transceiver select.
TERMSEL	Output	Termination select.
SUSPENDM	Output	Suspend mode indicator.
LINESTATE[1:0]	Input	Current state of D+; D-.
OPMODE[1:0]	Output	Operating mode selector
XDATAOUT[w–1:0]	Output	Data to be transmitted. Bus width 8 or 16-bit.
TXVALID,TXVALIDH	Output	Transmit data valid.
TXREADY	Input	Transmit data ready.
XDATAIN[w–1:0]	Input	Received data. Bus width 8 or 16-bit.
RXVALID,RXVALIDH	Input	Receive data valid..
RXACTIVE	Input	Indicates that a valid packet is being received.
RXERROR	Input	Indicates error in Rx packet.
DRVVBUS	Output	VBus power enable.
CHRGVBUS	Output	Charge VBus.
DISCHRGVBUS	Output	Discharge Vbus.
VBUSVALID	Input	VBus compared to selected VBus Valid threshold.
AVALID	Input	VBus compared to 'A' Session Valid threshold.
SESSEND	Input	VBus compared to Session End threshold.
HOSTDISCON	Input	*(Host mode)* Indicates if peripheral is attached.
DPPULLDOWN	Output	Enable for a pull-down resistor on the D+ line.
DMPULLDOWN	Output	Enable for a pull-down resistor on the D– line.
IDDIG	Input	MUSBMHDRC Connector ID.
IDPULLUP	Output	Enable for associated pull-up resistor.
VSTATUS[statbits-1:0]	Input	PHY Status data – *if implemented.*
VCONTROL[cntlbits-1:0]	Output	PHY Control data – *if implemented.*
VCONTROLLOADM	Output	Control data read enable – *if implemented.*
CPU INTERFACE SIGNALS (AMBA AHB Slave)		
AHB_HSEL	Input	AHB select..
AHB_HREADYI	Input	AHB ready input.
AHB_HREADYO	Output	AHB ready output.
AHB_HSIZE[1:0]	Input	AHB transfer size.
AHB_HTRANS[1:0]	Input	AHB transfer type.
AHB_HADDR[9:0]	Input	AHB address bus.
AHB_HWDATA[31:0]	Input	AHB write data bus.
AHB_HRDATA[31:0]	Output	AHB read data bus.
AHB_HWRITE	Input	AHB write not read.
MC_NINT	Output	CPU interrupt. Active low.
RAM INTERFACE SIGNALS		
RAM_ADDR[ramw–1:0]	Output	RAM address bus.
RAM_DATAI[31:0]	Input	RAM data input bus.
RAM_DATAO[31:0]	Output	RAM data output bus.
RAM_NCE	Output	RAM select. Active low.
RAM_NWR	Output	RAM write enable. Active low.
SYSTEM SIGNALS		
CLK	Input	System clock. Must be greater than 30MHz.
NRST	Input	Power-up reset. Active low.
TM1	Input	Test Mode support.
USB_NRSTO	Output	USB function reset output. Active low.
SOF_PULSE	Output	Frame Sync Pulse.
DMA_REQ[eps–3:0]	Output	DMA endpoint requests.
NRSTA	Input	Asynchronous reset.
NRSTO	Output	Power-up reset synced with CLK
NRSTXO	Output	Power-up reset synced without XCLK

The mode initially selected depends on the state of the ID line from the USB mini-A/B connector through which the core is attached to the other device. If sampling the ID line identifies the core as the "A" device, the core will initially go into Host mode. If the core is identified as the "B" device, it will initially select Peripheral mode.

The MUSBMHDRC supports Host Negotiation Protocol (HNP), so where it is connected to another dual-role controller, it can switch roles between host and peripheral. It also supports Session Request Protocol (SRP), whereby the "B" device can request a session by pulsing first the data line and then VBus.

Details of both these protocols are given in the *USB On-The-Go* supplement to the USB 2.0 specification.

Multi-Point Operation

In a multi-point set-up, the MUSBMHDRC acts as the host to a range of USB peripheral devices connected to the MUSBMHDRC via one or more USB 2.0 or USB 1.1 hubs. Hi-, Full-, and Low-Speed transactions are supported through a USB 1.1 hub.

The key feature here is the way target device functions can be allocated to the core's individual Rx and Tx endpoints, just by recording the function address and, where necessary, the relevant hub address and port details. Further, this allocation can be made dynamically, allowing the system designer to make full use of the endpoints to service the needs of the different devices that are attached to the core.

Once this information has been recorded, transactions can essentially be carried out as if to a single target device, though there are some additional steps to take where the endpoints are allocated dynamically and where control transactions are handled other than through the core's endpoint 0 (EP0).

Transaction scheduling is carried out in hardware. The software used just needs to ensure that it does not try to open more pipes than can be supported by the available bandwidth.

Reference Technology Gate Count:

- 2Tx+Rx Endpoints: 42,000 gates

- w/Dynamic FIFO Sizing: 49,500 gates

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