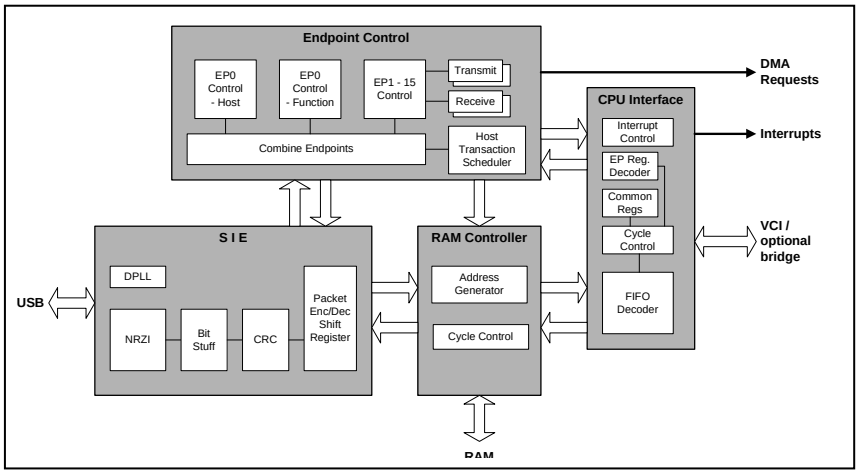
Inventra™ MUSBFDRC
USB Full-Speed Dual-Role Controller

Soft Core (RTL IP)

D A T A S H E E T



MUSBFDRC Block Diagram

Overview

The Inventra MUSBFDRC primarily provides a 'Dual-role' USB controller for use as either the host or the peripheral in point-to-point communications with another USB function (which may be either full-speed or low-speed). Alternatively it can be used as the function controller for a full-speed USB peripheral.

It complies with both the USB standard for full-speed functions and the *On-The-Go* supplement to the USB 2.0 specification. The *USB On-The-Go* specification has been introduced to provide a low-cost connectivity solution for consumer portable devices such as mobile phones, PDAs, digital still cameras and MP3 players. Devices that are solely peripherals initiate transfers through a Session Request Protocol (SRP) while Dual-role devices support both SRP and Host Negotiation Protocol (HNP).

The MUSBFDRC is user-configurable for up to 15 'Transmit' endpoints and/or up to 15 'Receive' endpoints in addition to Endpoint 0, individually programmable for Bulk/Interrupt or Isochronous transfers.

Access to the FIFOs associated with these endpoints and to the internal control/status registers is either via an 8-bit PVCI-compatible synchronous CPU interface or via an optional 32-bit MUSBFDRC – AMBA AHB bridge. There is also support for DMA access to the Endpoint FIFOs, including a DMA controller built into the AMBA–AHB bridge. This bridge also supports multi-layer operations.

The MUSBFDRC doesn't itself include any RAM for these FIFOs – this RAM needs to be added by the user. The RAM interface offered by the core is configurable for endpoint FIFO sizes from 8 bytes to 2048 bytes (except for the Endpoint 0 FIFO which is fixed at 64 bytes.)

A graphical user interface is provided for configuring the core to the user's requirements. An estimate of the gate count for the selected configuration is displayed on the configuration screen.

Major Product Features:

- Operates either as a function controller for a USB peripheral or as the host/peripheral in point-to-point communications with another USB function
- Complies with the USB standard for full-speed (12 Mbps) functions and with the *On-The-Go* supplement to the USB 2.0 specification
- Supports point-to-point communications with one full-speed or low-speed device
- Supports both Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- Standard Device Requests handled efficiently in software for flexibility
- Supports Suspend and Resume signaling
- Configurable for up to 15 additional Transmit endpoints and up to 15 additional Receive endpoints
- Configurable FIFOs, with option of dynamic FIFO sizing
- Synchronous RAM interface for FIFOs
- Support for DMA access to FIFOs
- Built-in PVCI*-compatible CPU I/F, optional AMBA™ AHB bridge offering DMA controller and support for multi-layer operations
- Performs all transaction scheduling in hardware
- Graphical User Interface provided for core configuration

Deliverables:

- Verilog and VHDL RTL source code
- Synthesis script for Design Compiler
- Verilog and VHDL testbenches
- Reference technology netlist
- Product Specification & User Guide

* Peripheral Virtual Component Interface, as defined by VSIA (OCB 2 v1.0)

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Modes of Operation

The MUSBFDRC has two main modes of operation – Peripheral mode and Host mode.

When acting as a peripheral, the MUSBFDRC provides all the encoding, decoding and checking needed in sending and receiving USB packets – interrupting the CPU only when endpoint data has been successfully transferred.

When acting as a host, the MUSBFDRC additionally maintains a frame counter and automatically schedules SOF, Isochronous, Interrupt and Bulk transfers. It also includes support for the Session Request and Host Negotiation Protocols required for point-to-point communications, details of which are given in the *USB On-The-Go* supplement to the USB 2.0 specification.

Whether the MUSBFDRC initially operates in Host mode or in Peripheral mode depends on whether it is being used in an 'A' device or a 'B' device. When the MUSBFDRC is operating as an 'A' device, it is initially configured to operate in Host mode. When operating as a 'B' device, the MUSBFDRC is initially configured to operate in Peripheral mode. The MUSBFDRC determines whether it is the 'A' device by monitoring the CID input, which should be connected to the ID pin on the mini-AB receptacle.

Session Request (SRP)

A session is defined as the period when VBus is on. VBus is always supplied by the 'A' device on the bus. Sessions can be started by the CPU associated with either an 'A' device or a 'B' device setting the Session bit in the DevCtl register. Where the 'B' device wishes to start the session, it will first try pulsing the data line, then pulsing VBus to wake the 'A' device. Sessions are ended by the CPU clearing the Session bit.

Host Negotiation (HNP)

When the MUSBFDRC is the 'A' device, it automatically enters Host mode when a session starts. When the MUSBFDRC is the 'B' device, it automatically enters Peripheral mode when a session starts. The CPU can however request that the MUSBFDRC becomes the Host by setting the Host Req bit in the DevCtl register. Host Negotiation is then conducted using the defined protocol when the MUSBFDRC next enters Suspend mode.

Reference Technology Gate Count: 6200 + 1500/1600 per each additional Tx/Rx endpoint (or 2500/2600 per endpoint if dynamic FIFO sizing required)

Signal Description

The MUSBFDRC has a maximum of 115 external signals: 35 inputs and 80 outputs.

USB INTERFACE SIGNALS		
SIGNAL	**TYPE**	**DESCRIPTION**
DIP	Input	D+ single-ended input.
DIM	Input	D- single-ended input.
DIDIF	Input	Differential input.
DOP	Output	D+ output.
DOM	Output	D- output.
NDOE	Output	Output enable for DOP, DOM. Active low.
SPEED	Output	Transceiver operating speed: Full-/Low-speed.
PUCON	Output	Connect pull-up resistor to D+.
PDCON	Output	Connect pull-down resistor to D+.
VBUSEN	Output	VBus power enable (for operation as 'A' device).
VBUSCHG	Output	Charge VBus (used when operating as 'B' device).
VBUSVAL	Input	VBus compared to selected VBus Valid threshold.
VBUSSES	Input	VBus compared to 'B' Session Valid threshold.
VBUSLO	Input	VBus compared to Session End threshold.
CID	Input	MUSBFDRC Connector ID. 1=B-type, 0=A-type.
IDEN	Output	Enable for sampling ID line (allows power saving).
CPU INTERFACE SIGNALS		
MC_ADDR[5:0]	Input	Address bus.
MC_DI[7:0]	Input	Data bus input.
MC_DO[7:0]	Output	Data bus output.
MC_NOE	Output	Data bus output enable. Active low.
MC_VAL	Input	CPU access validate.
MC_RNW	Input	Read not write.
MC_ACK	Output	CPU access acknowledge.
MC_NINT	Output	CPU interrupt. Active low.
DMA_REQ[m:0]	Output	DMA endpoint requests, one for each endpoint.
DMA_NACK	Input	DMA Acknowledge. Active low.
RAM INTERFACE SIGNALS		
RAM_NCE	Output	RAM Enable. Active low.
RAM_ADDR[n:0]	Output	RAM address bus. Bus width is dependent on the number and type of endpoints configured.
RAM_DATAI[7:0]	Input	RAM data input bus.
RAM_DATAO[7:0]	Output	RAM data output bus.
RAM_NWR	Output	RAM write enable. Active low.
SYSTEM SIGNALS		
FCLK	Input	Input clock. This clock should be 48 MHz.
CLKOUT	Output	System clock output (12 MHz).
CLK	Input	Buffered version of the CLKOUT clock.
NRST	Input	Power-up reset. Active low.
USB_NRSTO	Output	USB function reset output.
SOF_PULSE	Output	Frame Sync Pulse.
USB_SUSPEND	Output	High when the MUSBFDRC is in Suspend mode.

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04/05 PD-40134.006a-FO