

Dynamic compact models of cooling mounts for fast board level design

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Abstract

Traditional board level thermal simulators provide temperature distribution on the board only. Recently developed simulators calculate exact junction temperatures obtained by the co-simulation of the detailed board model and the dynamic compact models of the devices on the board. The DELPHI project targeted the generation of steady-state compact models while the aim of the recent PROFIT project was the same for dynamic simulations. This paper tries to extend the DELPHI and PROFIT methodologies to allow completing dynamic compact models of device packages with compact models of cooling assemblies for the same purpose: co-simulation with the detailed board model. A few case studies are presented showing how such models can be constructed using structure functions and transient model fitting tools.

Objectives

With the always growing speed and density of electronic appliances their thermal characterization is becoming a key task in thermal engineering. There is an emerging demand from system level designers on fast and accurate thermal simulators that are capable to predict junction temperatures quickly and accurately. Traditional board level simulators are capable to calculate temperature distribution on a printed board only. Latest thermal simulators also calculate the most critical parameter: the junction temperature of semiconductor devices inside the package [1]. This can be realized by a co-simulation of the detailed model of the board with the dynamic compact models of the device packages. (In this paper we prefer using the term ‘dynamic’ to indicate that the model describes both transient and frequency domain behavior.)

The hottest devices on the board are most likely equipped with some cooling mount (heat-sink, heat spreader, fan, etc.), thus, for accurate prediction of the junction temperature the compact model library of the thermal simulator should be completed with *compact models for cooling mounts*, too.

The aim of this paper is to present a methodology of creating compact models of different cooling assemblies for the application in fast board level thermal simulators.

Methodology for generating dynamic compact models

A comprehensive description of creating compact models is given in [2] and [9]. The usual way is the following:

1. A detailed model based on the physical structure is generated. This has to be analyzed by a field solver and validated against measurement results. An appropriate set of boundary conditions for measurement and analysis was defined in the DELPHI project [3].
2. A compact model is constructed as a network of a few thermal resistances and capacitances. This model inherits the "package faces" from the detailed model where the boundary conditions were applied. These are the "ports" of the compact model to be terminated by further model networks or appropriate boundary conditions when the model is used. The known compact model topologies are different regarding accuracy and boundary condition independence.
3. When the topology is fixed, the element values of the model are "tuned". As suggested in [4], it is useful to divide a large set of boundary conditions into two sets, a "model set" and a "test set". Parameter tuning means an optimization step where the response curves of the compact model are fitted to those of the detailed model, for all boundary conditions of the "model set". It is also shown in [9] that the accuracy is better if the "model set" contains the extreme conditions.
4. The *predictive power* of the generated model is evaluated: the response curves of the compact model are compared to those of the detailed model using the "test set" of the boundary conditions.

In our present approach we modify slightly the above process. We start from a series of thermal transient measurements with boundary conditions similar to those of the DELPHI method. Instead of setting up a detailed model as in step 1 above, we optimize the compact model directly, using the transient measurement results as input. We use

- one series of measurements as "model set" for generating the compact model for the *packaged device*,
- another independent "model set" series of measurements is used for characterizing the *cooling mount*. We use tuning methods for optimal fitting of both models.
- A third, independent series of measurements is used as "test set". Here the cooling mount is attached to the packaged device which was modeled in the first series.

- The models are accepted if the third measurement set and the compact model simulation using the "test set" boundary conditions correspond *without any further fitting*.

The method gives good results and it is easy to realize as long as the number of faces/ports is not very high, requiring many different measurements for all model and test boundary conditions. Generally, a proper blend of detailed model simulations and measurements validating each other is suggested.

Example I: Modeling a SOT-93 package and two different heat-sinks

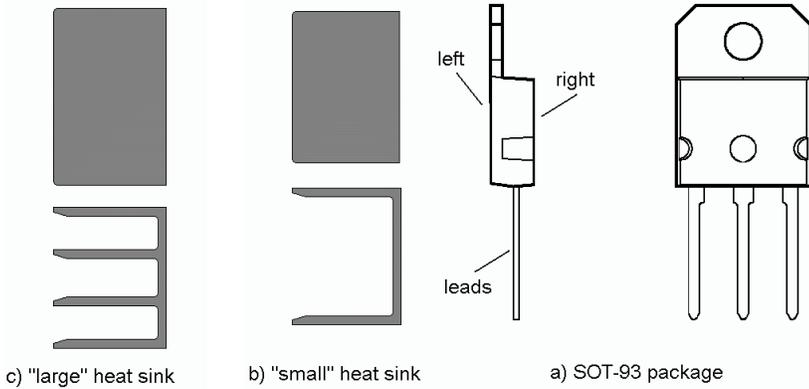


Figure 1 a) SOT-93 package. Characteristic faces where heat flow occurs are named left, right and leads.

b) The "small" heat sink. **c)** The "large" heat sink.

In this example we first set up a compact model for the SOT-93 package which is a popular choice for packaging three-pole power devices. Afterwards compact models for two different heat sinks are created. For the simplicity they are referred to as "small" and "large" below (Figure 1 a,b,c).

First measurement set - model set for package modeling

We used an NPN bipolar power transistor (BD245) packaged into the SOT-93 package. The characteristic faces of the package were named as *left*, *right* and *leads*.

The measurement was designed with boundary conditions similar to the DELPHI prescriptions. The measurement was carried out in a dual cold plate, with interface layers (Figure 2, Table 1). A power step of 12 W was applied and 100 sec of the thermal transient was captured real-time, with a high time resolution (1µsec) and high temperature resolution, measuring U_{EB} "on-the-fly" as described in [6]. Transient curves are shown in Figure 6. The measurement was followed by a post-processing step in the measurement software, which automatically generated descriptive functions of the packaged device, like:

- transient response curves
- time constant spectrum
- cumulative and differential structure functions

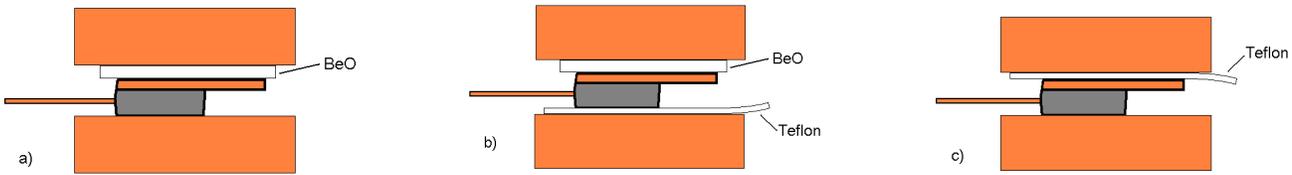


Figure 2 Dual cold plate measurements of the SOT-93 package: **a)** DCP1 **b)** DCP2 **c)** DCP3 setup

We used the DOTCOMP compact model generating tool [4] to optimize the model. The input data to this program have to be expressed as heat transfer coefficients (HTC) on characteristic faces and the total heat capacitance of the system. We found that the easiest way to create these input data is starting from the so called structure functions (cumulative and differential, widely published by Székely et al. [5] [6]).

These are nothing else than a graphic representation of the one dimensional equivalent (detailed) thermal RC network of the measured system (Figure 3). Moreover, heat transfer coefficients, thermal resistance and total system capacitance values can be directly read on them.

	width [mm]	nominal HTC [W/Km ²]	Rth [K/W] @ A=280 [mm ²]
BeO	0.72	3.8E+05	0.0095
Teflon	0.19	9.1E+02	3.9

Table 1: Interface layers used in the measurement setups of Figure 2

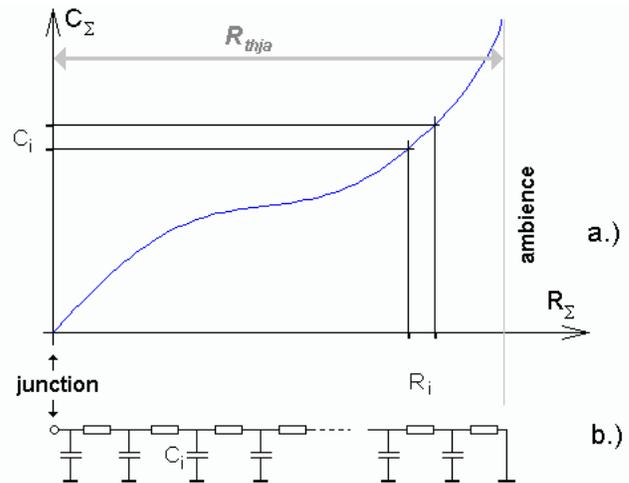


Figure 3 Cumulative structure function: the graphic representation of the thermal RC equivalent of the system

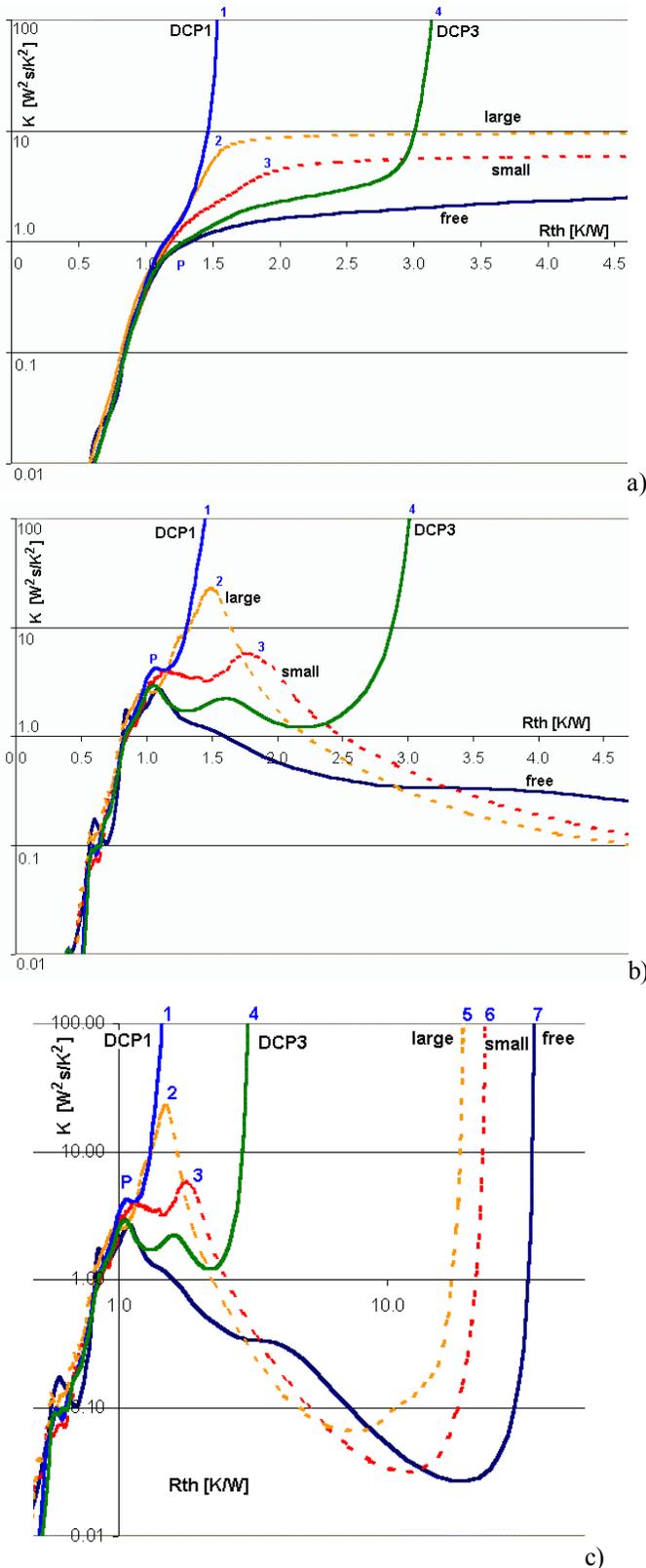


Figure 4 a) Cumulative structure functions of different thermal measurements on a BD245 transistor. DCP1 and DCP3 belong to the model set, large, small and free belong to the test set. **b), c)** differential structure functions

Figure 4 shows different structure functions. Curves DCP1 and DCP3 were derived from the transients of the corresponding dual cold plate measurements. The DCP2 curve runs very near to DCP1 and is not shown. Curves “large”, “small” and “free” were generated from still air measurements and will be discussed later as part of the third, “test” measurement set.

Figure 4a is the cumulative structure function [5] [6] and characterizes the thermal conductance path from the junction to the ambience. At low gradient sections a small amount of material having low capacitance causes large change in thermal resistance. These regions have low thermal conductivity or small cross-sectional area. Steep sections correspond to material regions of high thermal conductivity or large cross-sectional area. Sudden breaks of the slope belong to material or geometry changes.

It is easier to identify the interface between the sections using the derivative of the cumulative curve: the differential structure function (Figure 4 b and c shows different intervals of it). Here peaks correspond to regions of high thermal conductivity like a heat sink and valleys show regions of low thermal conductivity like die attach.

Characteristic points can be easily identified on the curves, these are points P, and 1 to 7. All curves nearly coincide from the junction to a peak near point P, this suggests that this is the junction-to-case section. One may object that instead of junction-to-case we should speak about different junction-to-face resistances. This is correct, and theoretically structure functions coincide only along the section of common heat flow. In case of this package there is a main heat flow path from the junction towards the copper base, which ends in the *left* face. The peak at P represents the mass of this copper base.

At the ambience the thermal capacitance grows to infinity, the position of 1 and 4 shows the junction-to-ambience values for DCP1 and DCP3. The measurement software enables easy interactive reading of point coordinates, partial thermal resistances between characteristic points etc. Using a material data library direct reading of area and volume values calculated from R_{th} and C_{th} values is also provided.

From the P point we get $R_{thP}=1.1$ K/W, and a cumulated capacitance for the whole package of $C_{thP}=0.9$ W^2s/K^2 . The distance of P to 1 along the x axis gives the case-to-coldplate thermal resistance for DCP1 which is $R_{th1}=0.45$ K/W (and practically the same for DCP2). The P to 4 distance gives $R_{th3}=2.0$ K/W for DCP3. From material

The DOTCOMP tool assumes a model topology suggested in [7] and shown in Figure 5a. The face-to-face (e.g. left-to-right) impedances are essential in modeling complex package structures because they provide higher accuracy and less dependence on boundary conditions.

The tool first requires the steady-state temperatures of the model set (right end of curves in Figure 6) and HTC values

parameters in Table 1 and physical dimensions we can calculate the effective heat transfer coefficients. The left face is approximately 280 mm^2 , and the right face is approximately 200 mm^2 . From R_{th1} and R_{th2} we get a HTC of 8000 W/Km^2 towards one side of the coldplate. This is much below the HTC of the BeO ceramics, so this value really shows the heat removal capability of the coldplate.

fitting means that despite this difference the measured and simulated transients look much the same.

Second, independent measurement set – model set for heat sink modeling

The two heat sinks of Figure 1 were characterized with the same technique. For the measurement of structure functions we needed a heat source and a fast sensor near to the source. So for simplicity the heat sinks were mounted onto another transistor, now in a small package (BD133). A power step of 0.5 W was applied, the measurements lasted for 1200 sec. Both heat sinks and a free standing transistor were measured in a still air chamber. Figure 8 presents the differential structure functions obtained for the three different cases.

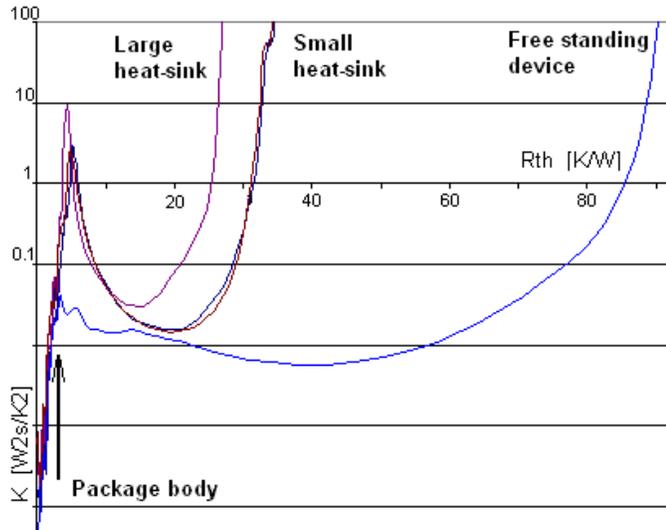


Figure 8 Differential structure functions: BD133 in free air and with the heat-sinks "small" and "large"

The simplest possible model is shown in Figure 9. Raw values of the model can be directly read from the structure function and are summarized in Table 3.

Of course, R1, C0 and C1 in Table 3 belong to the (very rough) model of the packaged heater device. We aim the correct fitting of the R2 value (which is approximately the case-to-sink_surface resistance), R3 value (which is equivalent of the sink_surface-to-ambient resistance due to natural convection), and C2 value, representing the mass of the heat sink

Simulation of this model network with the raw values gave a transient response, which resembled the measured curve but was far from perfect fitting.

Fitting one single element, the C2 capacitor, we got the curves of Figure 10 for the "small" heat sink and similar ones for the "large" heat sink. The match is very good after 1 second, where the time constant(s) of the heat sink dominate. Enhancing or tuning the transistor model would give better match for short times but this was not our target now.

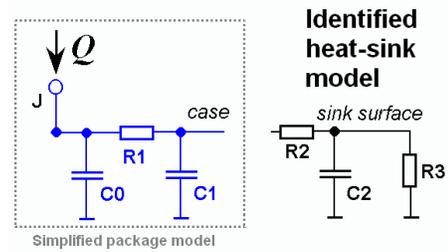


Figure 9 Simple model of a transistor with heat sink

	"small"			"large"			
R1	3.5	C0		R1	3.5	C0	
R2	1.8	C1	0.07	R2	1.0	C1	0.07
R3	28.7	C2,raw	1.73	R3	22.5	C2,raw	4.02
		C2,fit	3.12			C2,fit	7.81

Table 3: Element values of the simplified model of the test device and the "small" and "large" heat-sinks.

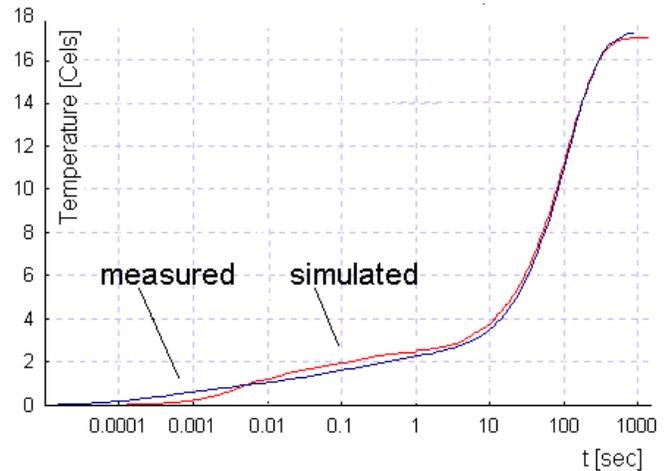


Figure 10 Measured and simulated junction temperature of a BD133 with the "small" heat sink

Third, independent measurement set – test set

The two heat sinks characterized in the second measurement set were mounted on the same BD245 transistor, which was used in the first measurement set. A power step of 1.5 W was applied, the measurements lasted for 1200 sec. Both heat sinks and a free standing transistor were measured in a still air chamber.

The resulting structure functions are shown in Figure 4 labeled as "small" and "large". The measured raw transients were compared to simulated transient responses where the SOT-93 model of Figure 5 and the heat-sink model of Figure 9 were joined. In the simulation port "left" of the transistor model was terminated by the heat-sink model, port "leads" was connected to the board and port "right" was left open. Figure 11 presents the obtained transients. Note, that the joint package-and-heat-sink model has never been fitted to the measurement results of the joint transistor-and-heat-sink

structure. The temperature responses of the junction match well, the models created can be accepted as good.

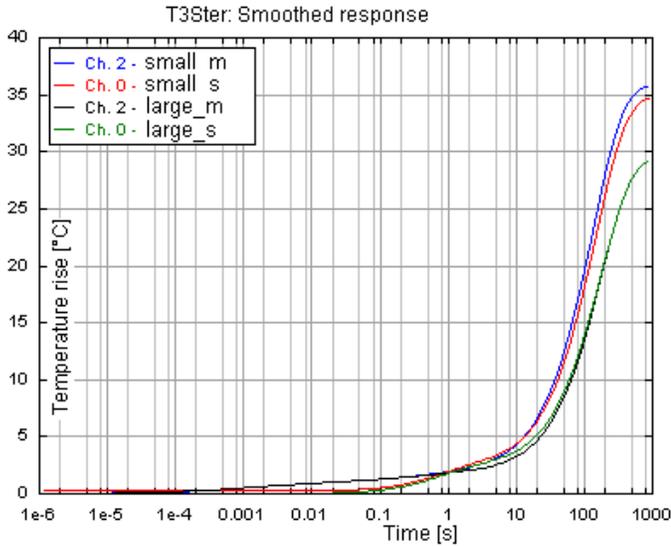


Figure 11 Non-fitted measurement and simulation results. Junction temperatures on the "small" and "large" heat sink mounted on SOT-93.

It has to be mentioned that heat sink performance in natural convection is very temperature and temperature-difference dependent. It is recommended to use more measured and simulated curves in all model and test sets, and to use "minimum", "typical" and "maximum" parameter sets for dynamic compact models in board simulations.

Using compact models of packages and cooling assemblies in board-level simulation

Once we have the methodology of creating dynamic compact *package* models as well as compact models of *cooling assemblies*, we can create model libraries for thermal simulators that can co-simulate the detailed model of a PWB and the attached compact device models. Figure 12 presents such a simulation concept [1]. The board model is populated with dynamic compact package models and some of them are "terminated" on their top surface with compact models of cooling mounts. The heat exchange between the packaged devices and the board takes place through the "footprints" of the packages. Further heat removal to the ambient can be modeled by heat transfer coefficients on the package surfaces (representing e.g. natural convection) or by the compact models of heat sinks.

In Figure 13 we present a simple model of a PGA package and cooling mount. The model library entry of the package is completed with the geometry of the footprints such as shown in Figure 14. Figure 15 shows a simple simulation example: a steady-state temperature distribution of a board with two such packages both dissipating 1W. The package on the right is equipped with a cooling mount, resulting in less heat transferred to the board and lower junction temperatures. The same behavior can be observed on junction temperature transients.

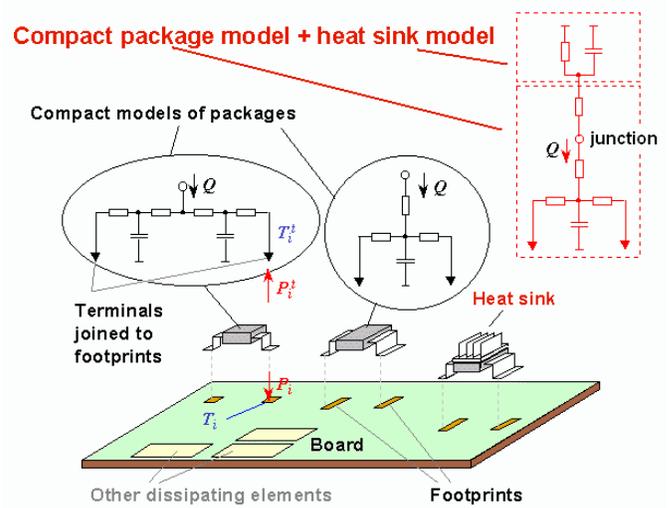


Figure 12 The concept of co-simulation of a detailed board model with dynamic compact models of packages and cooling assemblies such as heat-sinks

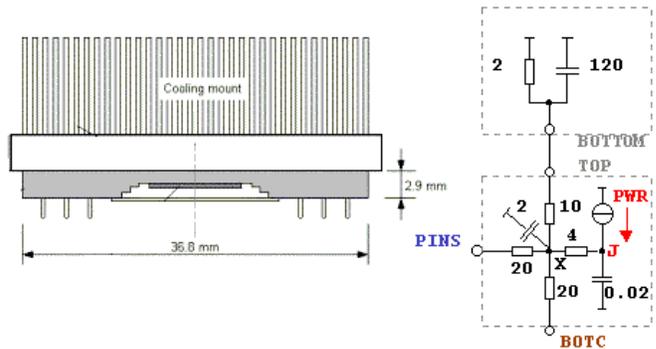


Figure 13 Compact model example of a PGA package and a finned cooling mount

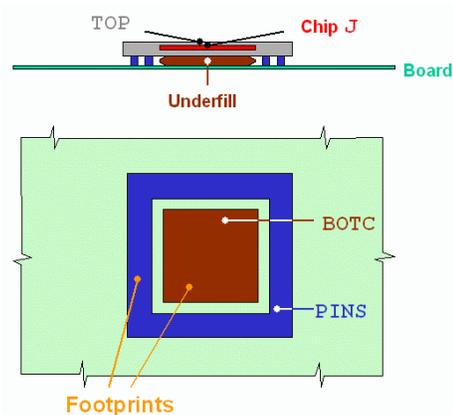


Figure 14 Footprint geometry of the PGA package shown in Figure 13

It is worth noting in Figure 16 that the initial parts of the simulated transients coincide for shorter times when the thermal wave propagates inside the package.

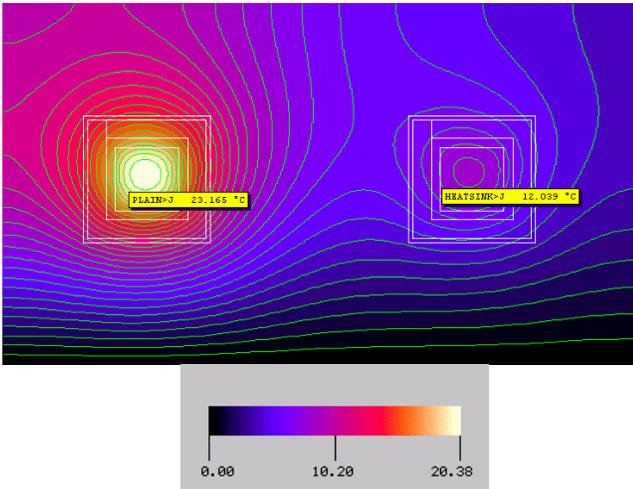


Figure 15 Steady-state temperature distribution of a PWB with two PGA models, and the junction temperatures. The package on the right has an attached heat-sink model as shown in Figure 13.

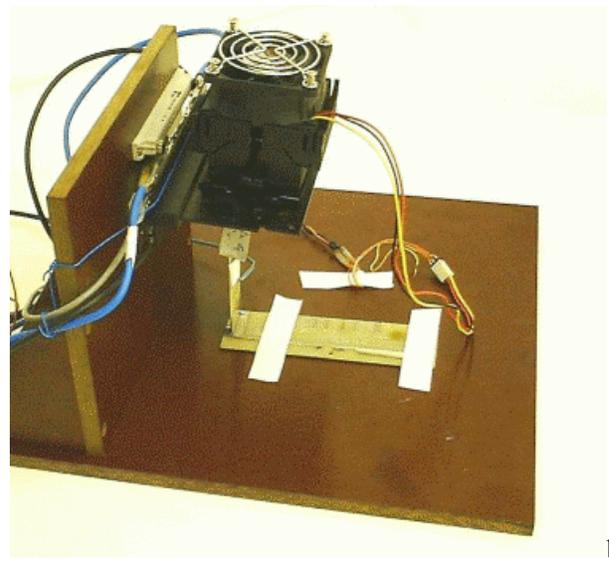
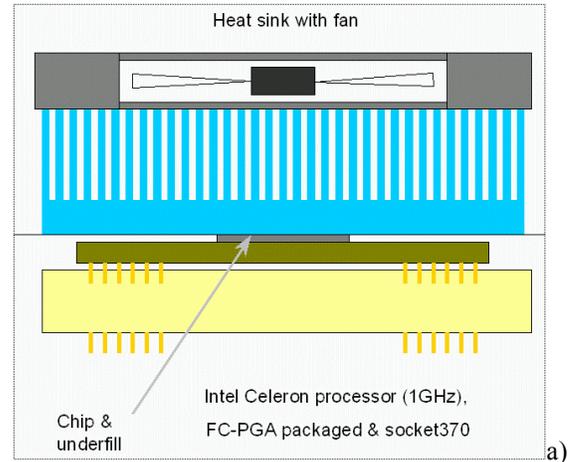


Figure 17 Device under test: a) schematic view of the processor+socket+cooling assembly, b) Measurement setup in a JEDEC 1 cubic foot chamber

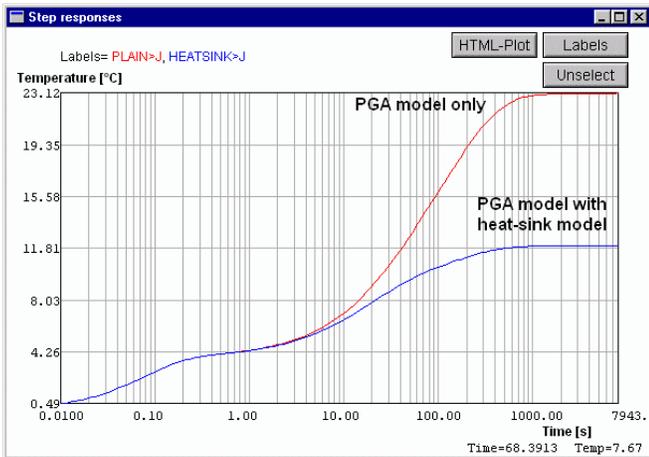


Figure 16 Thermal transient responses obtained by the two models as calculated by the THERMAN program [8].

Creating a model of a cooling assembly with a fan

As a case study on modeling cooling assemblies for up-to-date high performance chips, we created a package model and a heat sink model for an Intel Celeron processor (Figure 17a). The thermal transient measurements were carried out in a JEDEC standard one cubic foot chamber. We measured:

- thermal transients of the processor chip at low dissipation level (2W), with no cooling assembly
- thermal transients of the processor chip at high power level (18W) with the cooling assembly attached (photograph of DUT in Figure 17b), at different fan speeds (S1=5700 rpm, S2=2200 rpm and S3=1300 rpm).

We heated up the processor chip applying power on the reverse biased substrate diode inherently realized in all CMOS ICs. The heating up transients (Figure 18) were captured with the "on-the-fly" method using the processor's built in sensor diode.

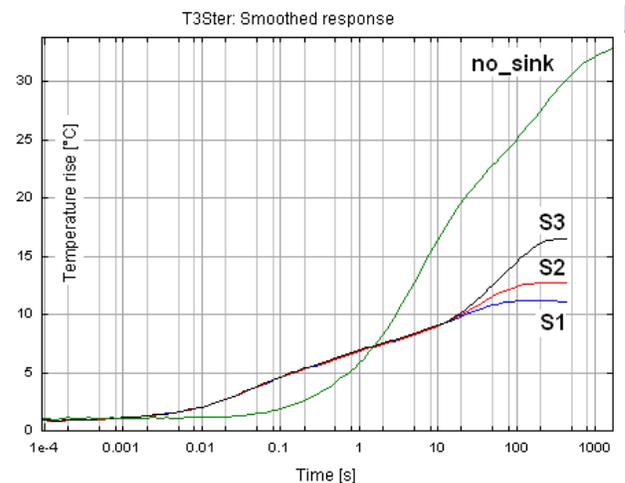


Figure 18 Measurement results for the DUT shown in Figure 17b for fan speeds S1, S2, S3 and without cooling assembly

Because of different power levels comparing the curves of Figure 18 is not easy. The structure functions, which are normalized by nature, were used for the identification of the heat sink model. In Figure 19 we can see the measurement of the case-to-ambient thermal resistance and the thermal capacitance of the heat sink.

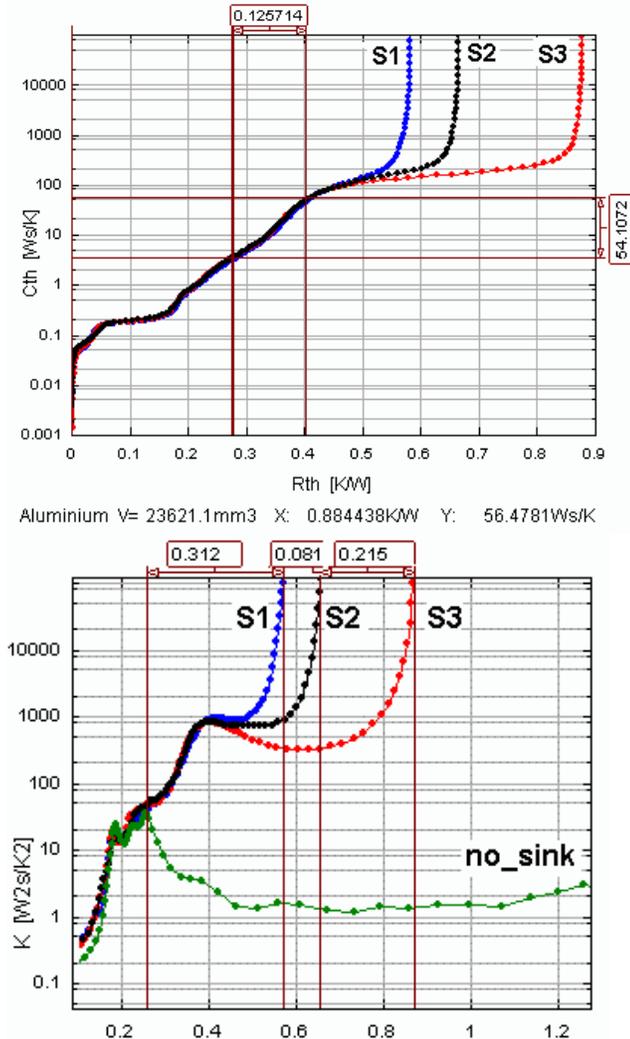


Figure 19 Structure functions of a Celeron processor with no heat sink and at different fan speed

In case of FC-PGA packaging only DCP2- and DCP4-like measurements are possible. Based on such measurements a dynamic compact model of the processor + socket couple was created, describing the situation without cooling assembly. The structure of the model was similar to the one described in the previous section. (A single TOP node at the rear of the processor chip was sufficient, but in this case we did not consider an underfill towards the motherboard of course.)

The model of the cooling assembly with a fan was created using the structure functions of Figure 19. Work is in progress to adapt parameterized cooling assembly models into our board simulator.

Conclusions

We have presented a methodology for creating compact models of packages and cooling mounts. The measurement and model identification technique for the package model was the one developed within the PROFIT project, while

models of cooling mounts are easily created from the structure functions derived by the evaluation of the measured high-resolution thermal transients.

The modeling approach presented here is another example of using *structure functions*: the major structural elements of the packaged device can be identified and the starting element values of a dynamic compact package model can also be found. Such package models can be fine-tuned by proper fitting tools. In case of cooling assemblies element values of a simple but sufficient compact model can be directly read from the structure functions that were obtained from measured thermal transient responses.

Similar transient measurements are used for a joint model verification of packages and attached cooling assemblies.

Attaching compact models of cooling assemblies to compact models of devices increases the accuracy of board-level simulators at virtually no cost in terms of CPU time, since during the co-simulation with the detailed model more than 99% of the CPU power is spent on solving the latter.

Acknowledgments

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References

- [1] M. Rencz et al.: Inclusion of RC compact models of packages into board level thermal simulation tools, Proc. of SEMITHERM XVII, San Jose, CA, pp 71-76 (2002)
- [2] C. Lasance: The Conceivable Accuracy of Experimental and Numerical Thermal Analyses of Electronic Systems, Appendix C, Proc. of SEMITHERM XVII, San Jose, CA, pp. 180-198 (2001)
- [3] C. Lasance et al.: A Novel Approach for the Thermal Characterization of Electronic Parts, Proc. of SEMITHERM XI, San Jose, CA, pp. 1-9 (1995)
- [4] C. Lasance, D. den Hertog, P. Stehouwer P: Creation and Evaluation of Compact Models for Thermal Characterisation Using Dedicated Optimisation Software, Proc. of SEMITHERM XV, San Diego, CA, pp. 189-200 (1999)
- [5] M. Rencz, et al.: Determining partial thermal resistances with transient measurements and using the method to detect die attach discontinuities, Proc. of SEMITHERM XVII, San Jose, CA, pp 15-20 (2002)
- [6] A. Poppe, V. Székely: Dynamic Temperature Measurements: Tools Providing a Look into Package and Mount Structures, Electr. Cooling Magazin, Vol. 8, No. 2, May 2002. www.electronics-cooling.com/html/2002_may_a1.html
- [7] H. Christiaens et al.: A Generic Methodology for Deriving Compact Dynamic Thermal Models, Applied to the PSGA package. IEEE Trans. On Components, Packaging and Manufact. Technology, Part A Vol 21, pp 565-576 (1998)
- [8] V. Székely et al.: THERMAN: a thermal simulation tool for IC chips, microstructures and PW boards. Microelectronics Reliability, Vol. 40, pp. 517-524 (2000)
- [9] C. Lasance: The Accuracy of BCI Compact Thermal Models for Non-Uniformly Distributed Boundary Conditions. Proc. 8th THERMINIC Workshop, pp. 251-259 (2002)