

# Multi-domain Simulation and Measurement of Power LED-s and Power LED Assemblies

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## Abstract

Besides their electrical properties the optical parameters of LEDs also depend on junction temperature. For this reason thermal characterization and thermal management plays important role in case of power LEDs, necessitating tools both for physical measurements and simulation. The focus of this paper is a combined electrical, thermal and optical characterization of such devices. In terms of simulation a novel approach of board-level electro-thermal simulation is presented whereas in terms of measurement, a combined thermal and radiometric characterization method is discussed.

## 1. Introduction

As it is well known the light output of LED-s strongly depends on the junction temperature: the total emitted optical power (Figure 1) and spectral properties (Figure 2) are both affected.

Temperature dependence of LED optical power at different current levels (IF, mA)

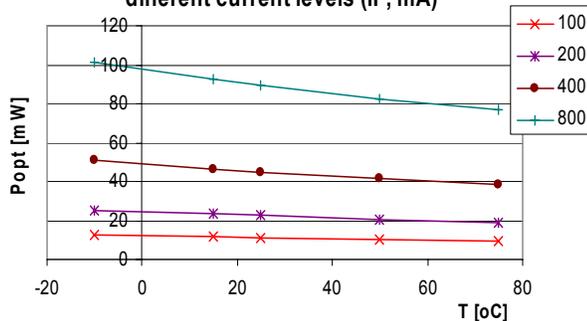


Figure 1: Temperature dependence of emitted optical power (radiometric flux) of a green power LED

This is an important issue at single power LED applications as well as in case of LED assemblies where a module realized on a metal-core PCB (MCPCB) contains multiple devices and the uniformity of the light output is important. To properly predict the electrical, thermal and optical properties of such (level 2) LED devices, a combined electrical-thermal and optical model of the packaged LED chips as well as proper modeling of the thermal environment of the single devices is needed. In our previous work we proposed a combined model of single, packaged power LEDs (level 1 devices) [1]. The sketch of such a model and its implementation is shown in Figure 3.

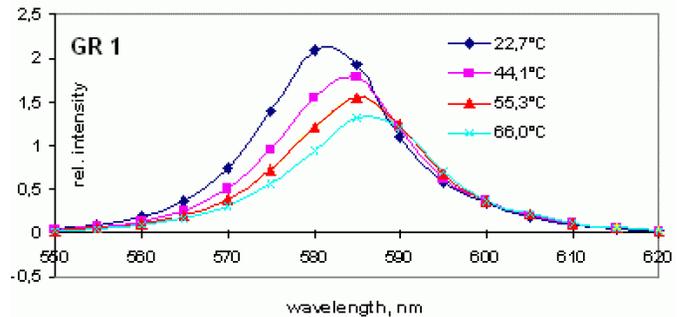


Figure 2: Temperature dependence of spectral properties of a green LED

In section 2 we describe our approach for the identification of the LED package thermal model directly from measurements. In section 3 we recall the basics of our electro-thermal simulator and its extension to board level simulations utilizing compact thermal models of packages. In section 4 we describe our multi-domain LED model and we conclude our paper in section 5 with an application example.

## 2. LED package compact thermal model directly from measurements

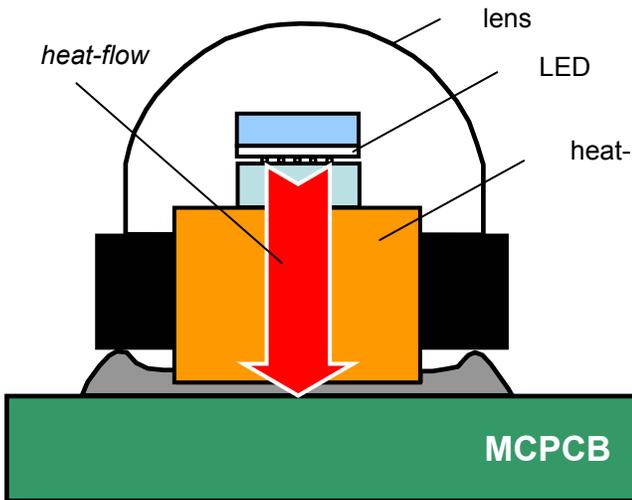
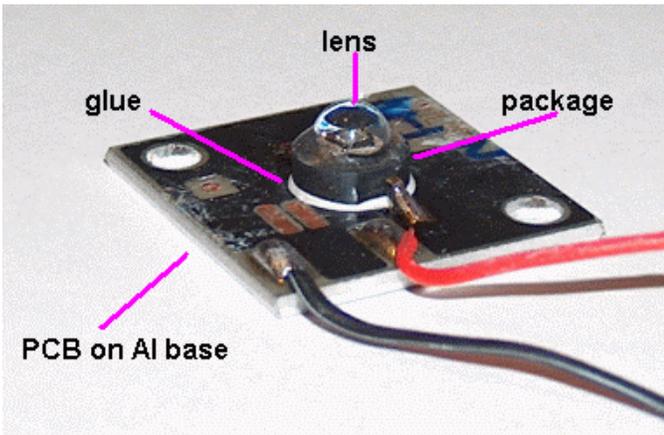
Creating compact thermal models (CTMs) of semiconductor device packages has been discussed in the literature for over a decade. Nowadays the DELPHI approach [2] is being widely accepted for creating boundary-condition independent steady-state CTMs, especially for IC packages. A natural extension of these CTMs is towards the transient behavior, in order to obtain dynamic compact thermal models (DCTMs). The methodology for creating such DCTMs as well as extending existing thermal simulators [3] for being able to handle such models was among the achievements of the PROFIT project [4].

In the DELPHI/PROFIT approach great emphases is put on boundary condition independence, since – especially in case of large area IC packages – there are multiple heat-flow path from the junction towards the ambient. Such models are obtained by simulation: a verified FEM model of the package is simulated with a so called *model set* of boundary conditions and the element values of a given model network are identified by an optimization method: the CTM is fitted to the simulation results of the detailed model. The "fitness" of the CTM is determined by applying a so called *test set* of boundary conditions. The CTM is accepted "good" if using the test set of boundary conditions its results match the results of the detailed model obtained for the same set of BCs.

When boundary condition independence of the CTM is not required, or there exists only a single junction-to-ambient heat-flow path realized by the package, the NID (network identification by deconvolution) method [6], [7] is a viable alternative.

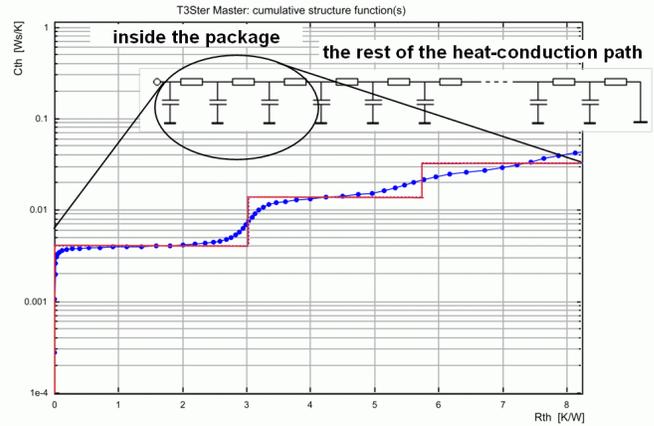
### 2.1. DCTMs of LED packages directly from measurement results

Having a closer look at a typical power LED package in a typical application environment (attached to metal-core PCB), one may easily conclude that in this case there is a single junction-to-ambient heat-flow path – see Figure 3. That is, a generic Cauer-type RC ladder model (Figure 4) would perfectly describe such a case, consequently, *structure functions* are also applicable in identifying a proper LED package model.



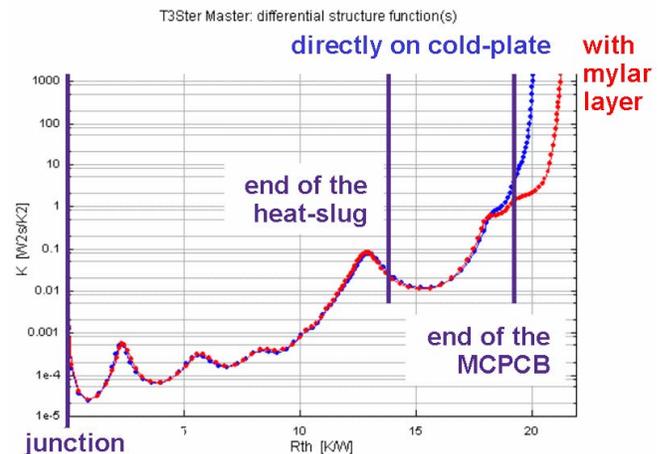
**Figure 3:** Junction-to-ambient heat-flow path in a typical power LED package attached to a metal core PCB

The element values of the Cauer-type DCTM of the LED package can be identified from a step-wise approximation of the *cumulative structure function* obtained directly from a thermal transient measurement of the package [8].



**Figure 4:** The step-wise approximation of the cumulative structure function of the package yields element values of a Cauer-type dynamic compact thermal model

Thermal transient measurement of level 2 devices (i.e assemblies either with a single LED like the one shown in Figure 3 or with multiple LEDs such as an RGB module like the one shown in Figure 12) typically takes place on a cold-plate. The measured thermal transients are converted into structure functions. The *differential structure functions* are used to differentiate between the various sections of the heat-flow path. In order to be able to find where the heat leaves the MCPCB, a simple technique is applied. Two measurements are carried out with two setups where the heat-flow path is allegedly changed at a certain location. Such a change must appear in the structure functions. For example in one setup the LED device is attached to the cold-plate directly while in a second measurement a thin *mylar* layer is inserted between the MCPCB and the cold-plate. This structural change is clearly shown by the differential structure functions: this way the end of the junction to-ambient heat-conduction path is identified (Figure 5).



**Figure 5:** Differential structure functions of level 2 LED assembly

Counting back from the ambient, the transition between the heat-slug and MCPCB can also be identified in these plots.

This is the location, where we can cut the Cauer-ladder obtained by the step-wise approximation of the cumulative structure function. This truncated ladder well describes the heat-flow path until the heat enters the MCPCB, thus, this model is suitable for considering the LED package during board level simulation. Further details regarding LED package level modeling can be found e.g. in [9].

## 2.2. Thermal and radiometric measurement of LEDs

Thermal transient measurements of semiconductor devices is based on the electrical test method [10]. In case of conventional devices calculating the thermal resistance (or thermal impedance for the dynamic case) is based on the measured temperature rise and supplied electrical power. In case of high power LEDs however, this method is not applicable, since about 20-40% of the supplied energy leaves the device in form of *light*. That is why we proposed a combined thermal and radiometric measurement setup [1] which in the meanwhile has been realized and used in this work.



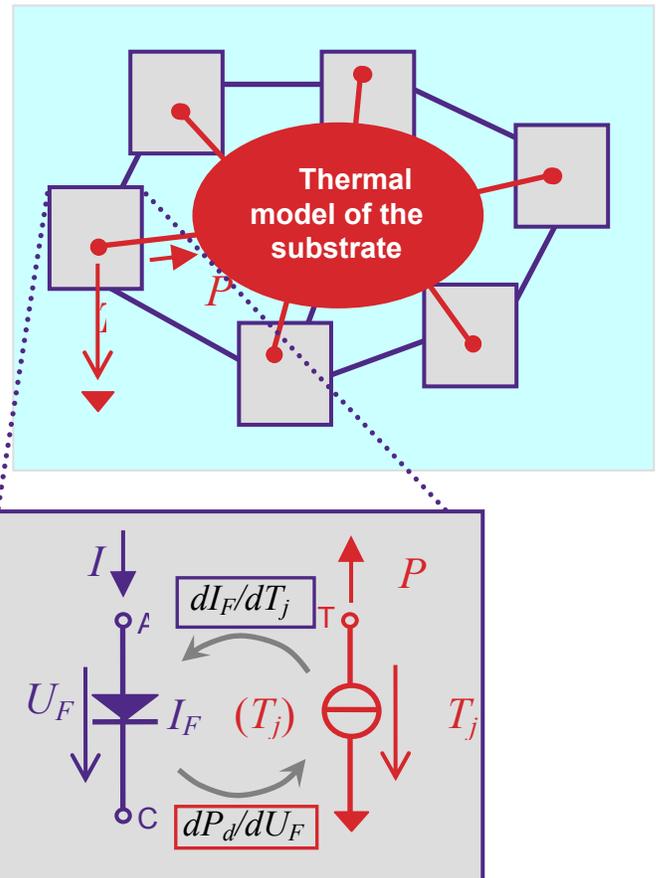
**Figure 6:** An automated photometric/radiometric measurement setup with a Peltier-cooled LED fixture, used in connection with the T3Ster thermal transient tester

The device under test is mounted to a Peltier-cooled fixture which is attached to an integrating sphere that is in compliance with the applicable standards and recommendations of CIE [11]. The Peltier-cooled fixture is used to stabilize the LED temperature for the optical measurements and it also serves as a cold-plate for thermal measurements. With a radiometric measurement performed in (thermal and electrical) steady-state of the LED/LED assembly under test, we can measure – among other parameters – the emitted optical power. Once all optical measurements are performed the DUT LED is switched off and we measure its cooling transient, using the T3Ster equipment of MicReD [12] in a usual diode measurement configuration. From the raw cooling transient we calculate the thermal impedance curve of the DUT, considering its emitted optical power. This impedance curve is converted into structure functions from which the CTM of the LED package is derived as discussed before.

Besides the combined thermal and radiometric measurement, temperature dependence of all parameters of the LED under test can also be measured, such as temperature dependence of the luminous flux, chromacity coordinates, wall plug efficiency as the electrical properties of the PN junction, providing input data for a Spice-like electro-thermal LED model.

## 3. Electro-thermal simulation on board level

### 3.1. Self-consistent electro-thermal simulation with simultaneous simulation



**Figure 7:** Sketch of a simple electro-thermal diode model with the  $N$ -port compact model of the substrate

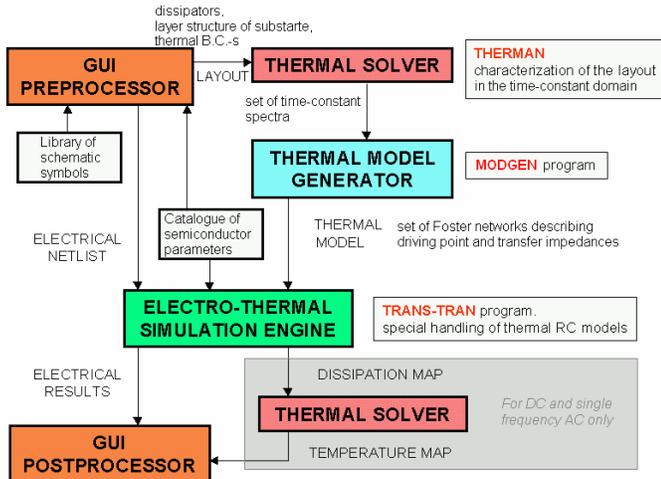
For electro-thermal simulation of electronic circuits containing semiconductor devices we use the *method of simultaneous iteration* [13], [14]. In this approach a *boundary condition dependent* compact thermal model of the substrate containing the active semiconductor devices is needed. This thermal network is solved together with the electrical one, simultaneously. The connection between the two networks is realized by the electro-thermal semiconductor device models: each device is completed with a thermal node (see Figure 7). The dissipation of the devices is fed through their thermal nodes into the thermal model network while the temperature at each device's thermal node is considered as individual device temperature. The parameters of the semiconductor device characteristics depend on these device temperatures, which are calculated as if they were electrical voltages – this

way maintaining the a self-consistent solution for the electro-thermal simulation problem [15], [16].

### 3.2. Compact thermal model of the substrate

The core of any electro-thermal circuit simulator using simultaneous iteration is how to generate and efficiently handle a boundary condition dependent dynamic compact thermal model of the substrate. This thermal model network can be considered as a thermal  $N$ -port – its ports are terminated by the thermal nodes of the semiconductor devices as shown in Figure 7. This  $N$ -port model is characterized by  $N$  driving point impedances describing heat removal from the given semiconductor directly to the ambient and  $N \times (N-1)$  transfer impedances describing the thermal coupling between any pair of devices on the same substrate.

The Network Identification by Deconvolution (NID) method uses the time- or frequency domain responses to generate the compact model [6], [17]. These responses can be calculated in advance, by using conventional thermal field-solvers. In our implementation we also use this approach. A very fast thermal simulator [18] provides the full set of  $N \times N$  time-constant spectra of all the thermal impedances of the substrate (driving point and transfer impedances). The time constant spectra are turned into RC Foster models of a few stages (as the accuracy requires) and these are simulated together with the electrical part in an efficient way [19].

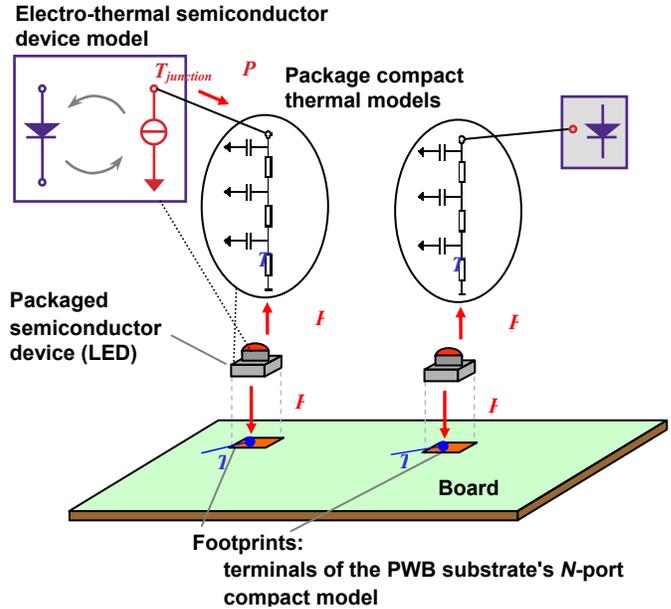


**Figure 8:** The simulation flow in our electro-thermal simulation system

### 3.3. Board level extension

The thermal time-constant spectra are automatically calculated by the thermal simulator for every dissipating shape of the circuit. This algorithm works well for die level IC simulation. In thermal simulation only mode, the applied thermal simulator already provides the option of using DCTMs of semiconductor device packages which are co-simulated with the detailed model of the PWB substrate [3]. The recent extension – as part of our new electro-thermal simulation environment [20] – was that now we can consider packaged semiconductor devices on any substrate with their DCTMs during electro-thermal simulation sessions as well. The  $N$ -port model of the substrate is calculated in the same way as for a die level problem. In case of packaged devices

considered with the DCTMs of their packages, the  $N$ -port compact thermal model of the substrate is extended for the footprint shapes as well. The DCTMs then are inserted between the corresponding footprint nodes of the substrate model and the junction thermal node of the electro-thermal device model (as shown in Figure 9) and are solved by the electro-thermal circuit simulation engine.



**Figure 9:** Electro-thermal model of a board level problem

### 4. Multi-domain LED model

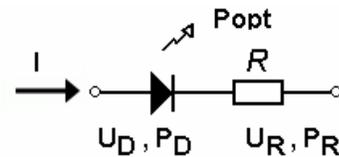
In case of light emitting diodes one has to subtract the emitted optical power from the supplied electrical power. This is the heating power that is fed into the package compact model:

$$P_{heat} = P_{el} - P_{opt} \quad (1)$$

In our prior study we have shown, that some of the LED devices may have a substantial dissipation across their electrical serial resistance [1] – see Figure 10. Thus, the total heating power is distributed between the junction and the series resistance:

$$P_{heat} = P_D - P_{opt} + P_R \quad (2)$$

where  $P_D$  denotes the electrical power dissipated on the junction and  $P_R$  is the power dissipated on the serial resistance.



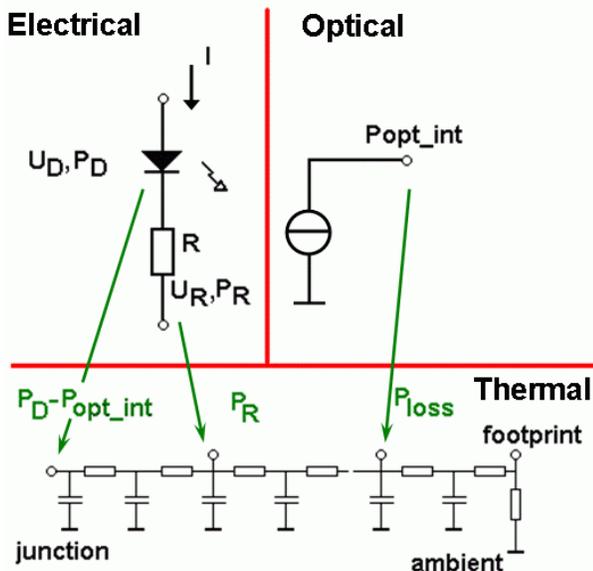
**Figure 10:** Model of an LED with large dissipation across its serial electrical resistance

The model parameters can be easily identified: combined measurements for obtaining  $P_{opt}$  were discussed in section

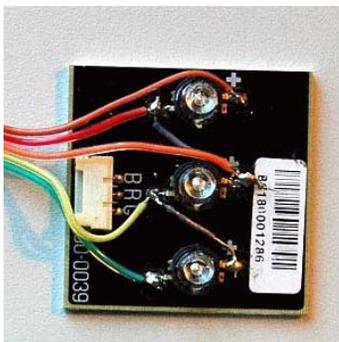
2.2, and the serial resistance of the device can be measured electrically in the same setup.

This serial resistance may be close to the junction, or might reside farther away from the junction, this way we can derive so called *hot resistor* or *cold resistor* type thermal models of an LED package. That is, the heat dissipated at the series resistance is fed into the junction-to-footprint heat-flow path either at the junction node, or further away, at a different node of the package model. This is a fact that one has to reflect in the electro-thermal LED model. Figure 11 presents the sketch of such a multi-domain LED model where a simple equivalent circuit model of the optical part is also included.

The emitted optical power (radiometric flux) can be calculated from the measured efficiency. One may consider optical losses inside the LED package that may also contribute to the heating of the device, but according to our experience its effect is negligible.



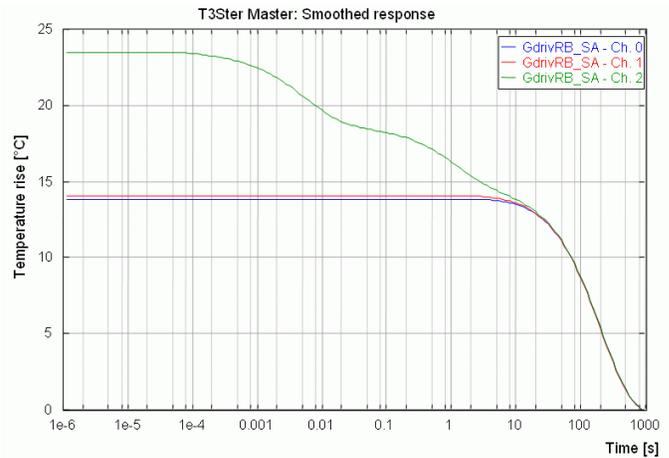
**Figure 11:** Multi-domain LED model, considering the electrical and thermal behavior and the emitted radiometric flux



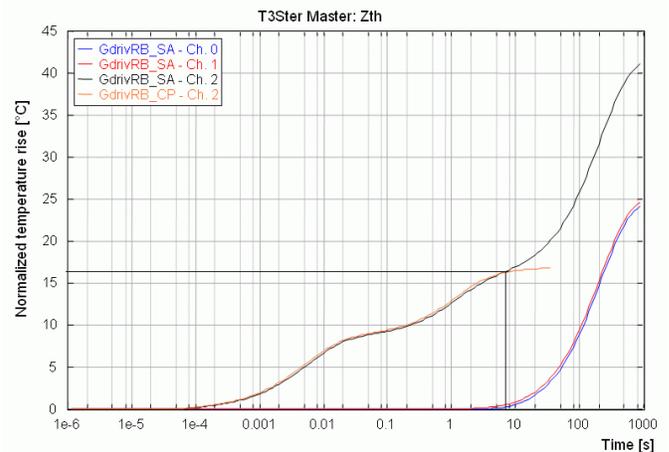
**Figure 12:** The investigated LED module

## 5. Application example

We have investigated the RGB LED module shown in Figure 12. All the three LEDs are in identical packages. In case of the green and blue LEDs of the module even the fine structures close to the junction are similar.



**Figure 13:** Cooling thermal transients measured in a JEDEC standard still-air environment (green LED driven, thermal response measured on all LEDs)



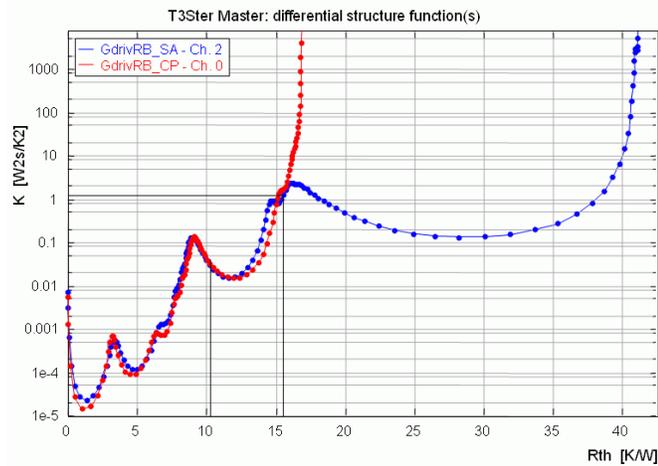
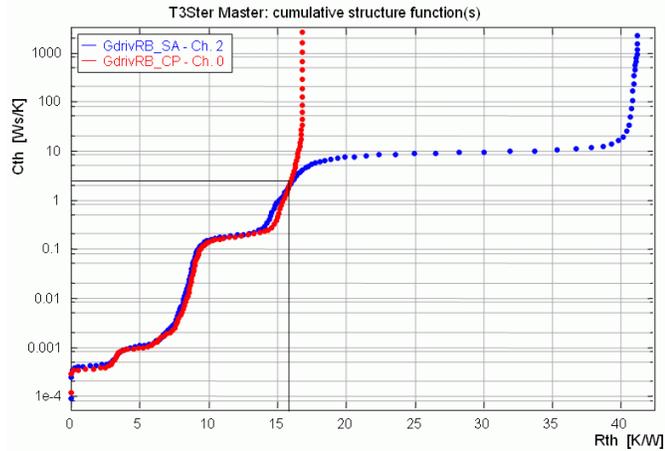
**Figure 14:** Cooling transient normalized to 1W – shown as thermal impedance curves. The driving point impedance of the green LED measured on cold-plate is also plotted

### 5.1. Measurements

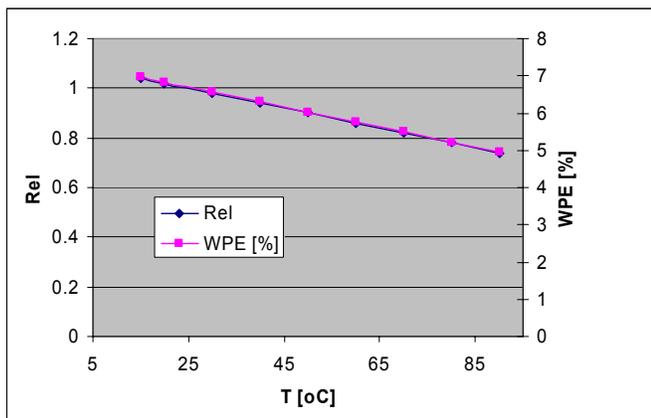
We carried out "plain" thermal transient measurements as well as combined thermal and radiometric ones. The thermal transient measurements were performed in a JEDEC standard still-air environment (Figure 13) as well as on cold-plate. If the driving point impedance curve measured on cold-plate is plotted with the ones measured in the still-air environment, one can easily see where do the two heat-flow paths corresponding to the two boundary conditions deviate (Figure 14). This measurement result supports our prior statement, that in this case of LED packages one may assume a single path from the junction towards the end of the heat-slug.

The same deviation (at around 15K/W cumulative thermal resistance from the junction) can be observed in the structure

functions. The measurements have also been carried out in the integrating sphere yielding efficiency data for the LEDs. Figure 16 shows the degradation of the efficiency of the green LED with increasing cold-plate temperature.



**Figure 15:** Cumulative and differentials structure functions for the still-air and cold-plate measurements



**Figure 16:** Cumulative and differential structure functions for the still-air and cold-plate measurements

The dynamic compact thermal model of the LED packages were identified according the procedure described in section 2.1 and was used in board-level simulations of the LED. The electrical part of the LED model was the standard LED model

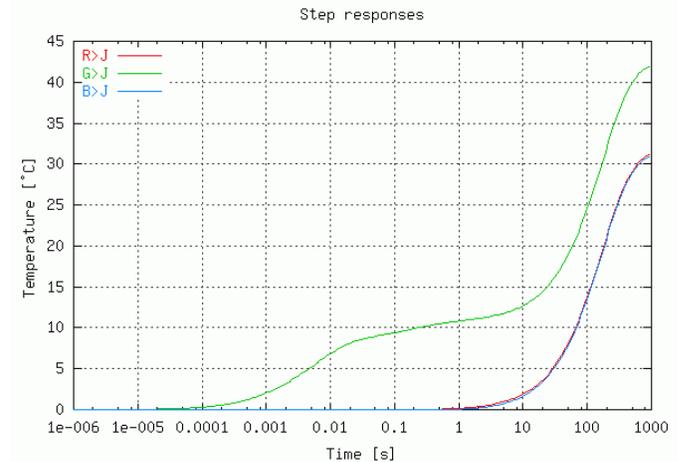
of our electro-thermal circuit simulation engine, parameterized for the actual LED devices.

The Spice model cards of a 5 stage RC model of the LED package are shown below:

```
.SUBCKT LADDER 1 0
C0 1 0 3.644748e-004
R0 1 2 3.178814e+000
C1 2 0 5.871133e-004
R1 2 3 3.125115e+000
C2 3 0 1.036391e-003
R2 3 4 1.605481e+000
C3 4 0 7.580729e-003
R3 4 5 9.286101e-001
C4 5 0 8.746424e-002
R4 5 6 1.113263e+000
.ENDS LADDER
```

## 5.2. Simulation

We created the thermal model of the LED module. We had to be satisfied with a Cartesian geometry – so circular footprints of the LEDs have been replaced with a 3x3mm rectangle. The Cauer-type RC ladder model shown in the above Spice netlist has been applied as the DCTM of our LED packages. Three LEDs have been placed onto an aluminum substrate of 30x30mm<sup>2</sup> area and 2.5mm thickness. Since the thermal model has been obtained from cold-plate measurements, we simulated the LED module in a still-air environment – for which we also had measurement results.

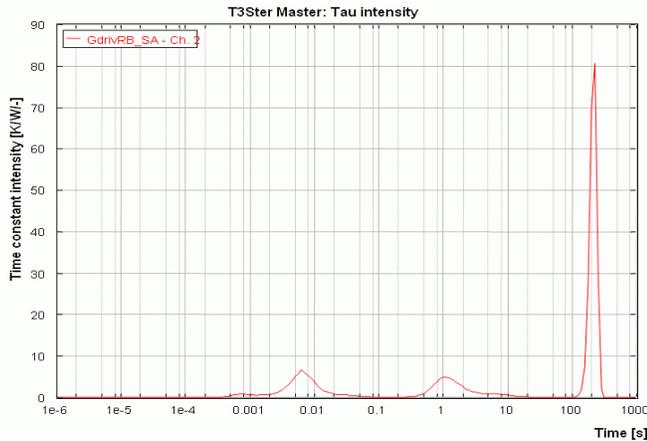


**Figure 17:** Thermal impedance curves at the three junction nodes of the investigated LED module, simulated in a still-air environment

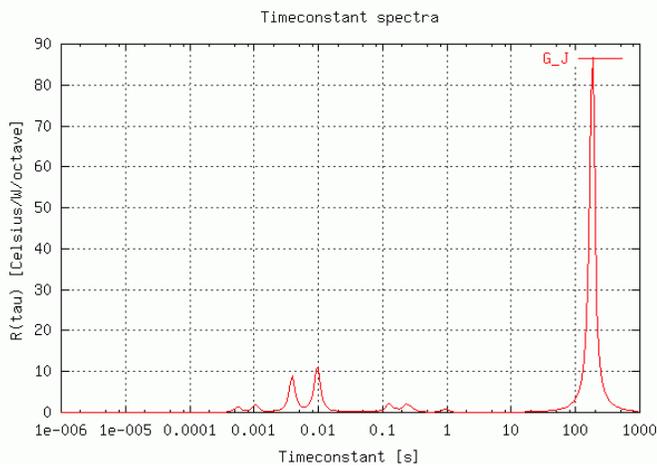
As one can see in Figure 17 the simulated thermal impedance curves agree well with the measured ones (Figure 14). The thermal delay between the green LED and the other two LEDs is also properly predicted by the simulation: the junction temperature of the blue and red LED starts to increase at about 1s.

The time constant spectrum of the driving point impedance (in this case the thermal impedance of the green LED) gives also a better image about the match of the simulation results and the measurement results. One can conclude from Figure 14 that time-constants corresponding to

structural elements inside the package should fall below 10s. Anything above 10s corresponds to the environment of the LED packages. In our case this means the metal core PCB in the still-air chamber.



**Figure 18:** Measured time-constant spectrum of the driving point thermal impedance of the RGB LED module when the green LED was heated



**Figure 19:** Simulated time-constant spectrum of the driving point thermal impedance of the RGB LED module when the green LED was heated

Figure 18 shows the measured and Figure 19 presents the simulated time-constant spectrum of the LED module in a still-air environment. During the simulation the LED package was considered by its CTM while the MCPCB was described by a detailed model. The spectrum line at about 200s corresponds to the MCPCB in the still-air chamber. Both the location and the magnitude of this spectrum line is properly predicted. In the measurement results we can see a dominant time-constant at around 1s – this is somewhat under predicted by the CTM. The other major time-constant inside the package is shown by the measurement results at about 7-10ms. This appears in the simulated spectrum at a correct location and with more or less correct magnitude – but split into two lines. This is the result of the lumped model – the step-wise approximation of the cumulative structure function.

Note, that the compact thermal model of the LED package was identified from thermal transient measurements carried out on a cold-plate but it has been successfully used to predict thermal behavior in a still-air environment.

## 6. Summary

In this paper we presented a measurement and simulation techniques for the multi-domain characterization of LED devices and LED assemblies. In terms of measurement we have been successfully using a combined thermal and radiometric measurement setup in order to be able to identify the actual thermal power that heats the junction of LED devices. The same measurement setup is also suitable to find the efficiency of the LEDs and to measure its basic electrical parameters – all as functions of temperature.

We have presented a compact model identification method which yield CTMs for LED packages directly from thermal transient measurement results.

Our die level electro-thermal simulation methodology has been extended to board level problems. The CTMs of LED packages have been successfully applied in a board level simulation problem.

## Acknowledgment

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## References

1. G. Farkas et al.: "Electric and thermal transient effects in high power optical devices" In proceedings of the 20th IEEE SEMI-THERM Symposium, 9-11 March 2004, San Jose, CA, USA, pp. 168-176
2. H. Rosten et al.: "Final report to SEMITHERM XIII on the European funded project DELPHI – the development of libraries for an integrated design environment", In proceedings of 13th IEEE SEMI-THERM Symposium, March 1997, Austin, TX, USA, pp. 73-91
3. M. Rencz, A. Poppe, V. Székely, B. Courtois: "Inclusion of RC compact models of packages into board level thermal simulation tools", in proceedings of the 18th IEEE SEMI-THERM Symposium, 11-14 March 2002, San Jose, CA, USA, pp. 71-76
4. C. Lasance: "Final report on the EC-funded thermal project PROFIT", in proceedings of the 9th THERMINIC Workshop, 24-26 September 2003, Aix-en-Provence, France, pp. 283-287
5. B. M. Guenin: "Embedded tutorial on the activities of the JEDEC JC15.1 Thermal Subcommittee", in proceedings of the 9th THERMINIC Workshop, 24-26 September 2003, Aix-en-Provence, France, pp. 291-293.
6. V. Székely: "THERMODEL: a tool for compact dynamic thermal model generation", in proceedings of the 2nd THERMINIC Workshop, 25-27 September 1996, Budapest, Hungary, pp. 21-26
7. V. Székely and Tran Van Bien: "Fine structure of heat flow path in semiconductor devices: a measurement and identification method", Solid-State Electronics, V31, pp.1363-1368 (1988)

8. P. Szabó et al.: "Thermal modelling of multiple die packages", in proceedings of EPTC 2005, 7-9 December 2005, Singapore, Volume 2, pp. 521-525.
9. J. H. Yu, G. Farkas, Q. van Voorst Vader: "Transient thermal analysis of power LEDs at package and board level", in proceedings of the 11th THERMINIC Workshop, 28-30 September 2005, Belgirate, Italy, pp. 244-248
10. Integrated Circuits Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device) EIA/JEDEC JSD51-1 standard.  
<http://www.jedec.org/download/search/jesd51-1.pdf>
11. <http://www.cie.co.at/publ/list.html#standard>
12. [www.micred.com/t3ster.html](http://www.micred.com/t3ster.html)
13. V. Székely: "Accurate calculation of device heat dynamics: a special feature of the Trans-Tran circuit analysis program", Electronics Letters, Vol 9, no.6, pp. 132-134 (1973)
14. G. Diegele et al. "Fully coupled Dynamic Electro-Thermal Simulation" IEEE Transactions on VLSI Systems, 5(3):250-257, 1997
15. V. Székely et al. "Self-consistent electro-thermal simulation: fundamentals and practice" Microelectronics Journal, 28:247-262, 1997.
16. V. Székely et.al.: "Electro-thermal and logi-thermal simulation of VLSI designs", IEEE Transactions on VLSI Systems, 5(3):258-269, 1997
17. V. Székely: Identification of RC Networks by Deconvolution: Chances and Limits, IEEE Transactions on Circuits and Systems-I. Theory and Applications, CAS-45(3):244-258, 1998
18. V. Székely, A. Poppe, M. Rencz, M. Rosental, T. Teszéri: THERMAN: a thermal simulation tool for IC chips, microstructures and PW boards. Microelectronics Reliability, Vol. 40, pp. 517-524, 2000
19. M. Rencz et al.: "Electro-thermal simulation for the prediction of chip operation within the package", in proceedings of the 19th IEEE SEMI-THERM Symposium, 11-13 March, 2003, San Jose, CA, USA, pp. 168-175
20. Gy. Horváth, A. Poppe: "The Sissy electro-thermal simulation system – based on modern software technologies", in proceedings of the 11th THERMINIC Workshop, 28-30 September 2005, Belgirate, Italy, pp. 51-54