

Structure function evaluation of stacked dies

Marta Rencz*, Vladimir Székely**

*MicReD Ltd, Hungary

** Budapest University of Technology and Economics, Hungary

rencz@micred.com

Abstract

In this paper simulation experiments demonstrate, that the structure function evaluation of the thermal transient testing is capable to locate die attach failure(s) of stacked die packages. The strength and the location of the die attach failure may be determined with the methodology of a fast thermal transient measurement and the subsequent computer evaluation. The special advantage of the methodology is that normally it does not require any additional circuit elements on any of the dies of the stacked die structure. The paper demonstrates the feasibility of the method both for stacked die structures of the same die size, and for pyramidal stacked die packages.

Keywords

Thermal transient testing, die attach quality, structure function, reliability testing

Introduction

The thermal qualification of stacked dies is an unsolved problem today. In case of stacked dies the die attach quality control problem is multiplied: the structure contains as many die attach layers as the number of chips, which are very difficult to test, resulting in pronounced reliability concerns.

It has been presented in earlier papers that the *Structure functions* [1], obtainable from the thermal transient measurements are applicable to indicate the die attach failures of single die packages [2]. In the paper of [2] die attach quality measurements on experimental ST-Microelectronics packages were presented. It was demonstrated that the presence of die attach voids in different forms and locations influences the thermal resistance of the glue layer such, that the voids in the die attach material can be conveniently detected with the help of fast thermal transient measurements and the subsequent evaluation. A special advantage of the applied structure function evaluation methodology is that it delivers not only the value but also the location of the increased thermal resistance in the heat flow path.

In the experiments presented in this paper we have examined whether the sensitivity of the methodology allows the application also in case of multiple die structures. Because of the extremely small thermal resistance value of the stacked dies it is not straightforward that the method can be used to uncover the location of die attach failures of stacked dies as well. And even if the method is applicable up to a certain number of dies, it has to be experimented what are the limits in the resolution of the method. It had to be also investigated

whether the methodology is applicable for stacked die structures of different die sizes as well.

In the rest of the paper we first give a short summary of the structure function evaluation methodology, presenting how can it be used to detect the thermal properties of various layers in the heat flow path. In the second part of the paper we show the results of our simulation experiments. These demonstrate the methodology is conveniently applicable to detect the location of die attach failures in stacked die structures of up to 4 silicon layers.

Theoretical background

The structure functions are obtained by direct mathematical transformations from the heating or cooling curves [1]. These curves may be obtained either from measurements or from the simulations of the detailed structural model of the heat flow path. In both cases a unit step function powering has been applied on the structure, and the resulting increase (or decrease, in case of switching off) in the temperature at the same location has to be measured in time, following the switching on.

The so-called *cumulative structure function* or *Protonotarios-Wing function* [3], gives the sum of the thermal capacitances C_{Σ} (cumulative thermal capacitance) in the function of the sum of the thermal resistances R_{Σ} (cumulative thermal resistance) of the thermal system, measured from the point of excitation towards the ambient, see Figure 1.

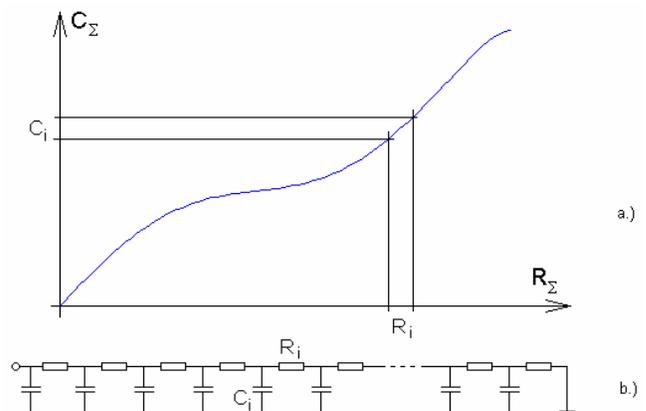


Figure 1 The cumulative structure function and the related Cauer equivalent circuit

The *differential structure function* is defined as the derivative of the cumulative thermal capacitance with respect to the cumulative thermal resistance, by

$$K(R_{\Sigma}) = \frac{dC_{\Sigma}}{dR_{\Sigma}} \quad (1)$$

Considering a dx wide slice of a single matter of cross section A , we can calculate this value. Since for this case $dC_S=cAdx$, and the resistance is $dR_S=dx/IA$, where c is the volumetric heat capacitance, I is the thermal conductivity and A is the cross sectional area of the heat flow, the K value of the differential structure function is

$$K(R_{\Sigma}) = \frac{cAdx}{dx/IA} = cIA^2 \quad (2)$$

This value is proportional to the c and I material parameters, and to the square of the cross sectional area of the heat flow, consequently it is related to the structure of the system. In other words: this function provides a map of the square of the heat current-flow cross section area as a function of the cumulative resistance. In these functions the local peaks indicate reaching new surfaces (materials) in the heat flow path, and their distance on the horizontal axis gives the partial thermal resistances between these surfaces. More precisely the peaks point usually to the middle of any new region where both the areas, perpendicular to the heat flow and the material are uniform.

Locating die attach failure on packaged stacked dies

In order to calculate the *structure function* of the heat flow path we need to simulate the thermal transient behavior, assuring one dimensional heat flow through the structure. In our simulation experiments this was obtained with the help of the SUNRED program [4], supposing cold plate at the header, and constant and evenly distributed dissipation was switched on the top of the structure. The increasing temperature was observed also on the location of the dissipation, on the top die.

Two different structures were investigated: a 3D package with equal size dies, and a pyramidal structure, that is frequently used in case of stacked die structures in order to facilitate the bonding.

Experiments on a parallelepiped structure

In the first simulation experiments 3, 2 and 1 dimensional simulations were applied for 3D stacked die structures of the same die size. In the 1 dimensional simulation we first created a one dimensional RC network model of the examined heat flow path, and we obtained the thermal transient curves of the structure from this network model by a circuit simulator.

We applied step function powering on the top surface of the top layer silicon, and simulated the resulting temperature transients in the structure by calculating the time dependent temperature in the middle of the top surface. In order to emulate measurement conditions we added random noise to the simulated results and used the same resolution (bit-number) in the results as we use normally in the measurements.

From the results of the simulated and measurement emulated transient response function, supposing one dimensional heat flow from the top surface of the stacked structure towards the cold plate we can calculate by direct mathematical transformations [5] the structure functions, that we normally obtain directly from the measured transient functions.

In the first group of the simulation experiments a stacked die structure of 4 dies with the same die size, same material parameters and thickness values were investigated. In these simulation experiments the dies are separated by die attach (glue) layers, that are supposed of having the same uniform thickness as the die thickness. The considered structure is presented in Figure 2. Note that the figure is strongly not to scale. The structure is in fact a very shallow structure, in which the heat is not spreading out uniformly in the silicon chips if cold plate is supposed under the structure.

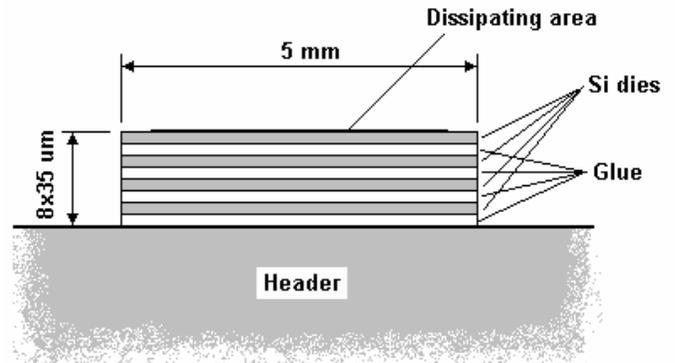


Figure 2 The simulated structure contained 4 silicon dies of 35mm thickness, separated by die attach of the same thickness. The figure is not to scale.

In Figure 3 the differential structure function of the structure of Figure 2 is presented, calculated from the simulated, but measurement emulated time response. The arrows are pointing to the peaks, representing the silicon dies, their respective distances on the horizontal axis give the values of the respective thermal resistances of the die attach material between them.

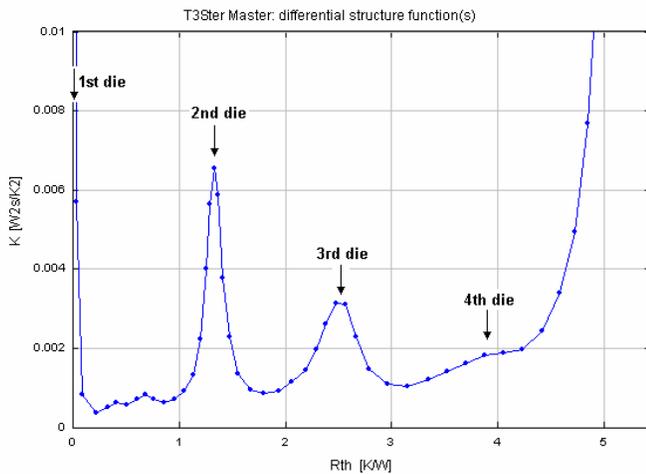


Figure 3 On the differential structure function of the structure the peaks represent the subsequent dies, their distances give the value of the die attach thermal resistance between them

In our first simulation experiment we have increased the thermal resistance of the die attach layer separating the 1st and the 2nd silicon dies, modeling a die attach void in between these dies. In Figure 4 from the shift in the right hand side end of the second curve we see the increased total thermal resistance of the structure, that is about 0.6K/W. A closer look of the two curves reveals even that, the location of the shift is at the die attach, between the first two silicon layers, resulting in an increased distance of the first two peaks.

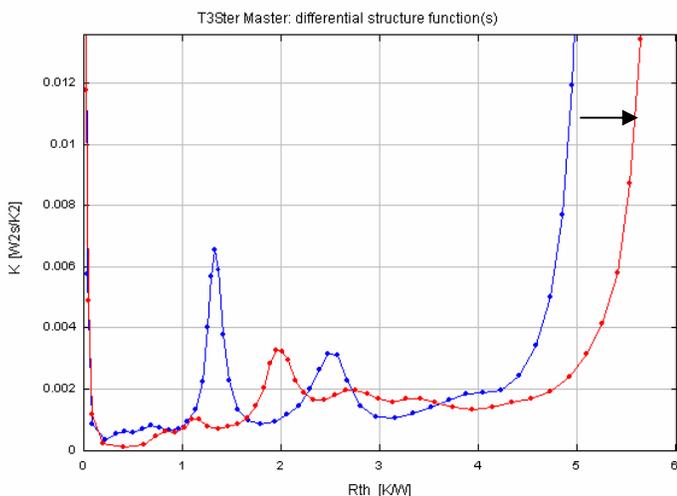


Figure 4 The increased thermal resistance of the die attach between the 1st and the 2nd silicon layer results in the displacement of the peak representing the 2nd die

In the second simulation experiment the same increased thermal resistance value was considered between the 2nd and the 3rd silicon dies. It is well observable from the comparison of the figures that the total thermal resistance of the structure is the same increased value in both cases, but the beginning of

the displacement is clearly distinguishable in both cases. In the second experiment the source of the increased thermal resistance is the die attach between the 2nd and the 3rd dies, since the first 2 peaks are at the same location in the differential structure function as in the case of the nominal curve of Figure 3.

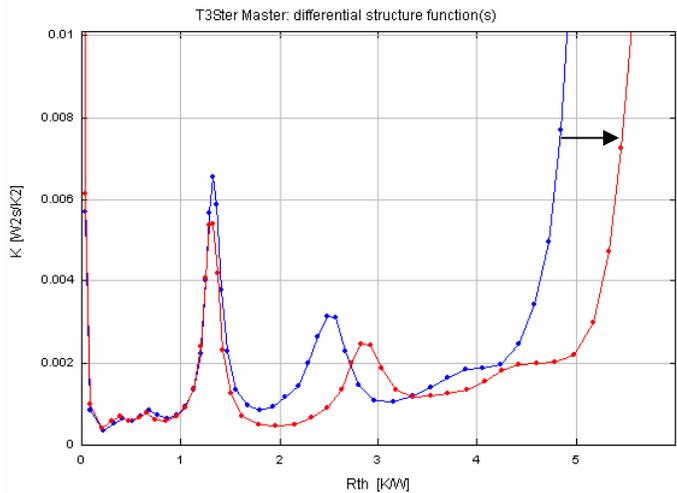


Figure 5 Inserting additional thermal resistance between the 2nd and the 3rd dies results in the shifting of the 3rd peak and from that on the whole right hand side of the curve

In our last experiment the same increased thermal resistance was considered between the 3rd and the 4th silicon dies. As it is shown in Figure 6 the total increase of the thermal resistance of the structure is the same as in the previous two cases, but the first 3 peaks did not move, so the source of the increase is between the 3rd and the 4th silicon layers.

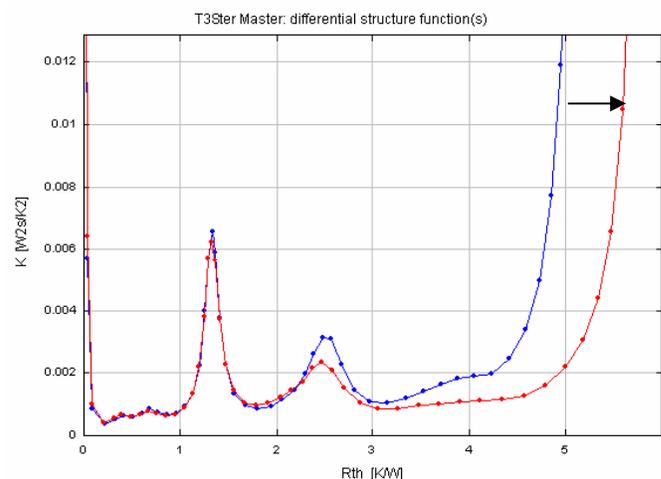


Figure 6 Inserting additional thermal resistance between the 3rd and the 4th dies results in the shifting of the 4th peak and from that on the whole right hand side of the curve

It is also observable from this figure, that this last peak is far not so pronounced as the first 3, suggesting that in these dimensions the examined 4 layer structure is about the limit of the resolution of the method.

Experiments on a pyramidal structure

One quarter of the investigated pyramidal structure is presented in Figure 7. The dissipating area was supposed in the middle of the top layer. Note, that the figure is not to scale.

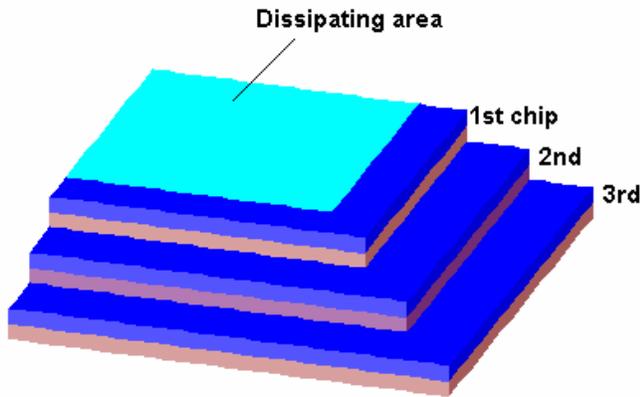


Figure 7 The investigated pyramidal structure

The sizes of the simulated structure were as follows. The size of the bottom die was 14x14 mm (7x7 in the ¼ simulation), the die size in the middle was 12x12 mm, and the size of the top die was 10x10 mm. The thickness of all the die and the glue layers were 0.035 mm. The considered thermal conductivity and volumetric thermal capacity values were 156 W/mK and $1.6 \cdot 10^6$ Ws/m³K for the silicon, 1W/mK and 10^6 Ws/m³K for the glue layers. The considered heat transfer coefficients were 6000 W/m²K on the bottom, and 100 W/m²K on the top.

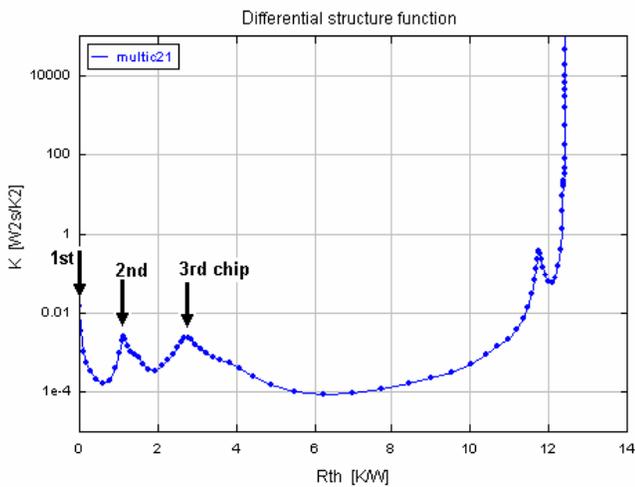


Figure 8 The structure function of the faultless pyramidal structure

The simulated time range was between 1 μsec– 2s, logarithmic time steps were applied, logarithmically equidistant 16 points/decade were calculated.

The differential structure function of the faultless structure shows the expected peaks, see Figure 8. The three chips and the glue under the structure can be well identified.

The thermal resistance and thermal capacitance values that can be read from the cumulative structure function of Figure 9 are good approximations of the real values, but do not give back exactly the values that can be calculated from the geometrical data. The explanation of this difference is that since the structure is very shallow, the heat is not spreading out in the whole silicon area. It is reaching the cold plate under the structure rapidly, and for this reason practically only the volume under the dissipating shape is participating in the heat conduction, showing smaller thermal capacitance values than expected.

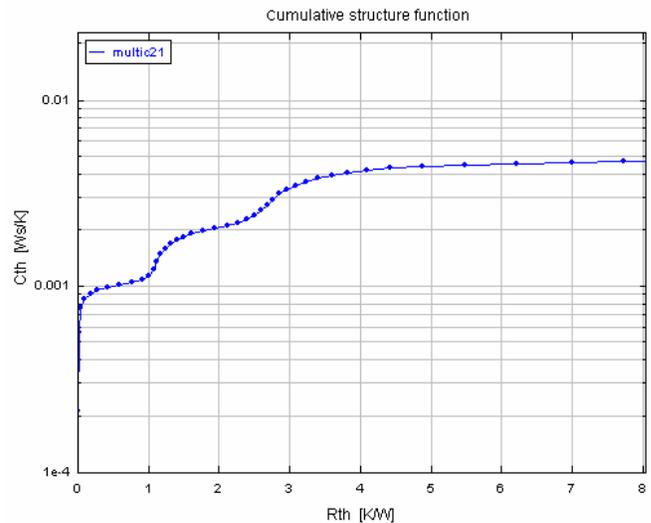


Figure 9 The cumulative structure function of the faultless structure

Let us suppose now die-attach failure between the 2nd and the 3rd chips. This can be modeled with an increased thermal resistance of the glue layer between these chips.

In the experiment presented in Figure 10 the thermal resistance of the glue between the 2nd and 3rd chips was increased by 33 %, that is, the thermal conductivity was decreased to 0.75 W/mK.

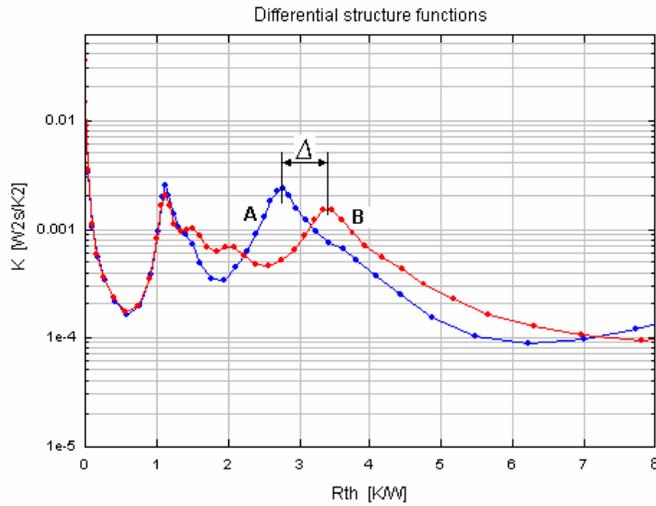


Figure 10 Die-attach voids are supposed between the 2nd and the 3rd chips. The displacement of the 3rd peak, that is, the distance between the A and B curves gives the increased thermal resistance.

The curve denoted by **A** in Figure 10 refers to the faultless case, **B** refers to the case of die attach void between the 2nd and 3rd chips. As it is shown in the figure, the peak referring to the 3rd chip is displaced now with the value of D , the peak referring to the 2nd chip did not move from the original position. The value of D gives back the increased thermal resistance of the glue layer, as expected.

In the next experiment the die-attach failure was supposed to be between the 1st and the 2nd dies. This was modeled by an increased thermal resistance again, obtained by decreasing the value of the glue thermal conductivity to 0.75 W/mK. The new results are presented in Figure 11. In this figure **A** denotes the faultless curve, **C** denotes the curve obtained by considering an increased thermal resistance between the 1st and 2nd dies. In this case, as it can be seen in the figure, the second peak is displaced, showing clearly the location of the increased glue thermal resistance, resulted from the die attach failure. The 3rd peak is displaced as well, with about the same value as the 2nd one.

From these simulation experiments we can determine that the location of an increased thermal resistance, even if this increase is not larger than 20-30%, may be determined also in the case of pyramidal die structures.

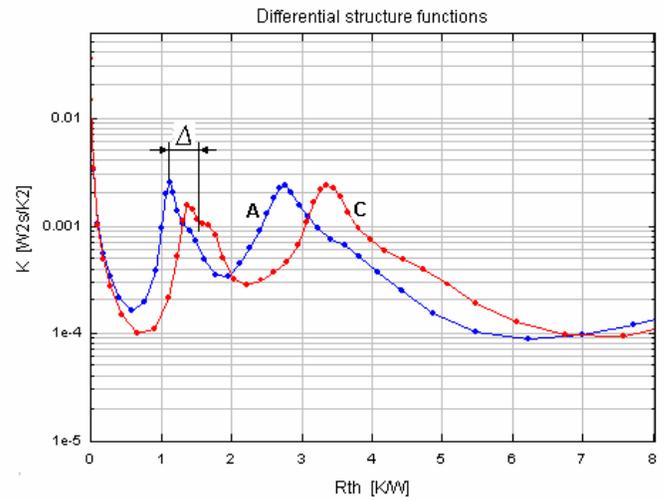


Figure 11 Die-attach voids are supposed between the 1st and the 2nd chips. The displacement of the 2nd peak, that is, the distance on the A and C curves gives the increased thermal resistance.

Conclusions

With the presented simulation experiments we have demonstrated the feasibility of locating die attach problems in stacked die structures. In the proposed methodology first the thermal transient response of the structure has to be obtained from measurement, and from this the differential structure function has to be calculated. Comparing the differential structure function of a measured sample with the differential structure function of a known good stacked structure, which can be obtained e.g. from the simulation of the structure, the differences can be easily observed. From the location of the shift in the structure function, in case of structures with die attach problems, the location of the die attach problem can be determined.

As the presented examples demonstrate the method works well both in the case of stacked dies of the same size, and in the case of pyramidal stacked die structures. In our investigations we examined structures that are similar to the ones realized and presented in the literature [6].

The resolution of the method will be further investigated with different die sizes and layer numbers, but from the simulation experiments up to now it can be expected that the method is well applicable for structures up to 4 layers of stacked dies.

We expect that at the time of presenting this paper we can present also measured results. But since in the whole process of the evaluation of the results *measurements* were emulated, we strongly believe in the applicability and the performance of the procedure.

For measuring the structure we do not need any extra elements on the dies if the substrate diodes of the individual dies are not connected electronically, since for the temperature sensing the substrate diode of the top die may be conveniently used. If for some reason the substrate diodes of the dies have to be connected electrically, other dedicated elements have to be selected on the dies for temperature sensing.

On the other hand, switching on either the whole dissipation on the top die, or just one dissipating element, may provide the constant source of heat during the time of the very short measurement. This means that obtaining the necessary transient curves is feasible normally without any special built in elements or test structures.

This way we may conclude that with the presented method the fast diagnosis of the die-attach problems of stacked dies is possible, and the method does not require any additional circuit elements in any of the stacked dies.

Acknowledgments

This work was supported by the PROFIT IST-1999-12529 Project of the EU and by the INFOTERM 2/018/2001 NKFP project of the Hungarian Government.

References

1. V. Székely and Tran Van Bien: "Fine structure of heat flow path in semiconductor devices: a measurement and identification method", *Solid-State Electronics*, V.31, pp. 1363-1368 (1988)
2. M. Rencz, V. Székely, A. Morelli, C. Villa: Determining partial thermal resistances with transient measurements and using the method to detect die attach discontinuities, SEMITHERM, March 1-14 2002, San Jose, CA, USA, Proceedings pp 15-20
3. E.N. Protonotarios, O. Wing: "Theory of nonuniform RC lines", *IEEE Trans. on Circuit Theory*, V.14, No.1, pp. 2-12 (1967)
4. V. Székely, A. Páhi, M. Rencz: SUNRED, a new field solving approach. *Symposium on Design, Test and Microfabrication of MEMS/MOEMS*, 30 March - 1 April, 1999, Paris, France, pp. 278-288
5. V. Székely: "A New Evaluation Method of Thermal Transient Measurement Results", *Microelectronics Journal*, Vol. 28, No. 3, pp. 277-292, 1997
6. C. Lin, S. Chiang, A. Yang: 3D stackable packages with bumpless interconnect technology, 5th Electronics Packaging Technology Conference, 10-12 December 2003, Singapore, 3002