

Thermal Simulation Reduces IC Cost by Comparing Flip-Chip/Wire Bond Thermal Performance

Early in the development process of a new dual-port 10 Gigabit Ethernet physical layer integrated circuit (IC), engineers at Applied Micro Circuits Corporation (AMCC®) faced a critical choice. The high performance chip presented thermal management challenges. AMCC engineers had to decide between a flip-chip package, which provides the optimal thermal performance, or a wire bond package, which is less expensive. They used Flomerics' Flotherm thermal simulation software to evaluate the thermal performance of the chip with each style of package. They determined that they could meet the thermal performance requirements with a less expensive wire bond package style. This choice reduced the cost of the new product, helping the QT2225/QT2225-1 ICs to provide the highest performance to price ratio of any product in its class.

AMCC originally targeted the QT2225/QT2225-1 at systems designers seeking higher densities for 10 Gbps applications including switches, routers and blade servers. Each device provides two 10 Gbps ports, enabling systems designers to reduce the number of chips by a factor of two. The QT2225-1 supports XFP modules and the QT2225 is ideal for high port density 10G datacom Ethernet switches, network interface cards, and telecom line card applications with SFP+ optical module requirements as well as for Backplane 10GBASE-KR support. "The new dual 10GbE QT2225 and QT2225-1 ICs demonstrate AMCC's commitment to the blade server and enterprise Ethernet markets by enabling our customers to leverage 10 Gigabit speeds over the backplane and higher port densities on the line card," said Neal Neslusan, Director of Marketing for AMCC.



Figure 1: AMCC's new QT2225.

Addressing thermal design early

Because AMCC operates at the leading edge of networking technology, the company long ago recognized the importance of addressing thermal management in the early stages of the design process. But the high-performance and high level of integration of this device presented greater than normal cooling challenges. AMCC Packaging Engineer Mark Patterson considered packaging alternatives at an early stage of the design process. A key question was whether a wire bond or flip-chip package would be used. In the flip-chip interconnection method the active area of the chip is flipped over downward so that any surface area can be used for interconnection. The flip-chip method allows for a large number of shorter interconnections which generally improves electrical and thermal performance. In the wire bond method, the die faces up and small pads of metal near their edges are attached to wires that lead to pins on the outside of the package. Wire bond interconnection offers a lower cost alternative in most applications.

The default way to evaluate the effect of different packages on the thermal performance of a new chip has long been to build a prototype of the package and chip and perform physical testing. This means that thermal performance evaluations cannot be initiated until prototypes are available, which sometimes delays the product introduction and nearly always limits the ability to optimize thermal performance by considering alternative packages.

Recognizing the importance of thermal management in pushing performance limits, a number of years ago AMCC began using thermal simulation software that makes it possible to produce detailed models that reconstruct the physical geometry of the package and accurately predict the temperature of the various elements within the package for a variety of conditions. The simulation results are used to evaluate the thermal performance of the device and provide thermal design guidelines to customers such as what volume and temperature of airflow is required to maintain junction temperatures at safe levels.

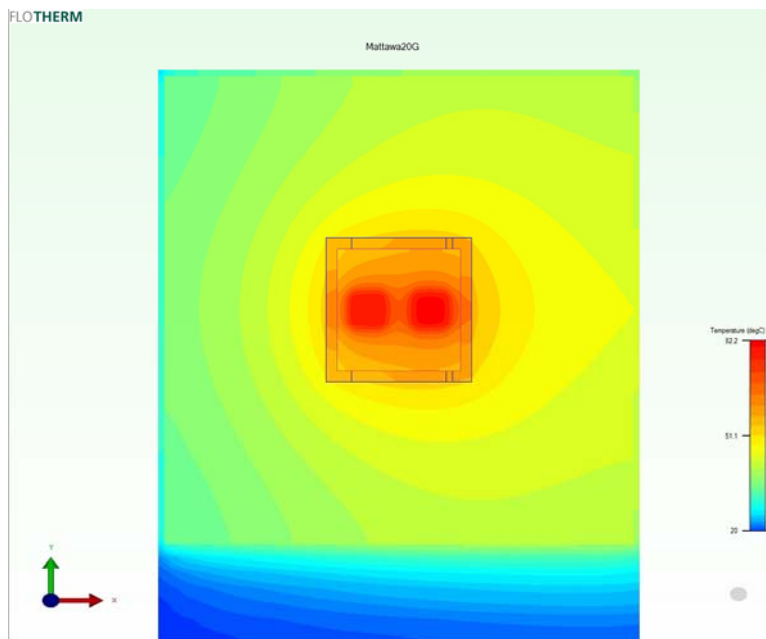


Figure 2: A surface temperature plot of the package as mounted on a thermal test board.

Reducing chip modeling time

Originally, maintaining the accuracy of the simulation required an intricate manual process that involves replicating the geometry of the die and package as well as lengthy simulations that are related to the complexity of the chip geometry. In the last several years, AMCC has taken advantage of new technology that reduces the amount of time required to simulate the thermal performance of new chip designs. The company utilizes Flomerics' Flopack website which greatly reduces the time required to model the thermal performance of chip designs. Users enter data describing the IC through forms using a Web browser and the website then creates a model of the device that can be incorporated into a thermal simulation. The user has the

choice of creating a full-detail geometric model or a behavioral compact model. Compact models can predict the temperature of electronic component packages at critical points such as the junction, case and board in far less time than is required with conventional detailed models.

“We use Flotherm for thermal simulation because it makes it easy and convenient to model different package styles and types,” Patterson said. “We simply enter the basic characteristics of the new chip into a form on the Flopack web site. The web site then generates either a geometric or a behavioral model of the chip. We can then modify the geometric model to account for detailed characteristics of the new chip and predict its thermal performance with a high level of accuracy. Later, we can convert the model to a compact form that accurately depicts the thermal performance of the chip while concealing our intellectual property. Most of our customers use Flotherm so it makes sense for us to generate the thermal model in a format that they can easily use in their own board- and system-level thermal simulations.”

Comparing flip-chip vs. wire bond

Patterson began the simulation process by using Flomerics’ Flopack website to create a model of the device using both types of packages. For each model he defined key parameters of the chip including the package type, package size, die size, number of balls, and number of metal layers in the package and power dissipation. The Flopack web site then created detailed thermal models of each type of package. Simulation accuracy was critical even at this early stage, so Patterson edited the models to more precisely match the company’s new device. Because he only had to make minor modifications, he was able to create the two models in a small fraction of the time that would have been required to model the geometry from scratch.

Patterson then inserted the models into a reference design that he frequently uses to test new ICs. The reference design passes a steady stream of air over the chip. He varied the temperature and volume of the airflow and the simulation results predicted the junction temperatures of the device. He tested each device at a range of 100 to 300 linear feet per minute and an ambient temperature of 85F. The simulation results showed that with either interconnection method the new parts would not exceed the junction temperature limits throughout the entire range of airflows. Patterson

validated the model by comparing the simulation predictions to physical testing results for similar products.

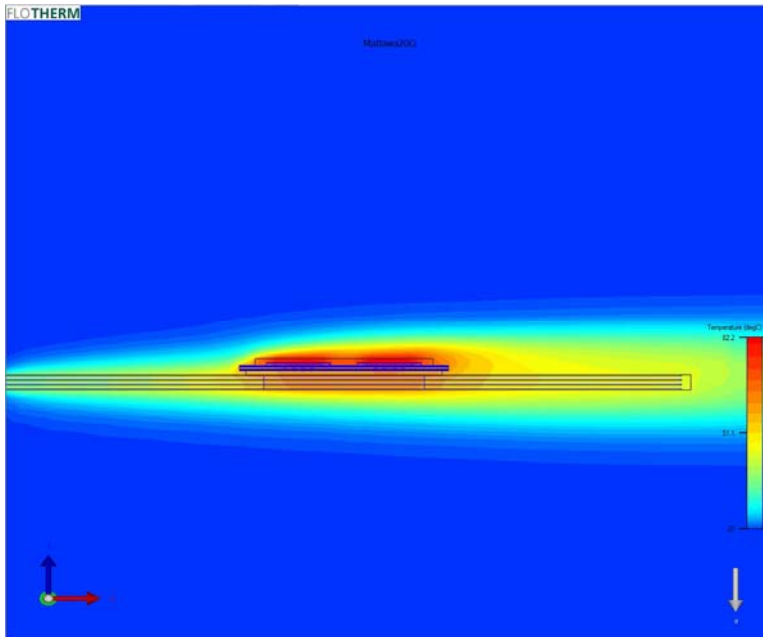


Figure 3: Side temperature profile through the package centerline.

Preparing design guides

On nearly every new product, AMCC also uses thermal simulation to create a design guide that provides customers with detailed thermal performance information under specified conditions. A typical design guide is a detailed engineering document that makes it clear to customers what is required to keep the chip cool under a wide range of conditions. This information enables them to make decisions in the early stages of their design process such as whether to work on improving the airflow over the chip or to use a heatsink.

AMCC also creates compact models for most of its products to provide a quick and simple prediction of the component's response to changes in airflow, temperature, and pressure. The models themselves provide basic thermal performance parameters under JEDEC standard boundary conditions. AMCC provides these models to customers who incorporate them into Flotherm models that they then use to predict the thermal performance of their complete systems. These models help ensure the accuracy of the customers' system-level models and also reduce the time needed to solve the system models.

“Thermal simulation helped us improve the performance to price ratio of the QT2225 and QT2225-1 by enabling us to optimize the tradeoff between thermal performance and packaging cost at any early stage of the design process,” Patterson concluded. “Software that can generate thermal models of ICs in less than an hour allows us to apply thermal simulation at an early stage of the design process. In this case we were able to substantially reduce the packaging cost as well as the design cycle for the cooling simulation tests. In nearly every product we make, we can verify the thermal performance of the device and generate design guidelines for customers.”

Flotherm software and the companion Flopack web site from Flomerics reduce the time and skill required to simulate complicated electronics cooling problems, because they are specially designed for electronic cooling applications. Flotherm and Flopack provide tools that allow users to assemble models from libraries, avoiding the need to create them from scratch. They provide an abundant supply of thermal model libraries for existing components. Flotherm provides an environment that enables fast, automated design studies. Automated gridding and distributed processing across networks streamlines the process of evaluating multiple iterations to optimize the design.