

Simulation Avoids Product Launch Delays

Integrated Device Technology (IDT) previously relied upon physical testing to ensure the thermal performance of the approximately 50 new products with new packaging configurations that it launches every year. Between 10% and 20% of the initial thermal designs did not meet specifications, requiring additional test iterations. In these cases, the product launch was typically delayed by about six weeks. Making a major change, such as switching to a different package type, at this stage also typically added engineering time and tooling costs.

More recently, IDT has begun simulating every new packaging configuration prior to physical testing with FloTHERM software from the Mentor Graphics Corp. Mechanical Analysis Division (formerly Flomerics). Using FloTHERM.PACK (online package model creation tool) makes it possible to create a model of a new package in about 30 minutes. IDT engineers usually evaluate the thermal performance of several different packaging alternatives in order to identify a package configuration that best meets thermal, board real-estate, cost and other objectives. "Since we have begun simulating every new packaging configuration, we have never had to make a late-stage design change nor has any product been delayed for thermal performance reasons," said Jitesh Shah, Advanced Packaging Engineer for IDT.

Integrated Device Technology develops mixed signal semiconductor solutions primarily used in digital media products. The company employs approximately 2,400 people worldwide and offers over 1,300 products in 15,000 configurations. IDT technology performs fundamental core tasks and functions such as offloading searches and table look ups to enable network and application-specific processors to operate more efficiently. IDT clocks, search engines and pre-processing switches handle the quality of service (QoS), prioritization and sourcing destination functionality that have historically been bottlenecks for processors. IDT switches allow higher-performance and lower-power blade servers to connect to whatever peripheral devices are needed to move digital media from one location to another.

Previous build and test method

In the past, IDT engineers tested products in a JEDEC standard environment to evaluate thermal performance of new packaging configurations. These tests were performed by mounting the packaged part on a JEDEC standard board and testing the assembly in natural convection and forced convection environments. A special thermal die with forward biased diodes designed on to it is used to measure the junction temperature in the packaged part. The cycle time for collecting each set of data was about 4 to 6 weeks involving design of the package and the board, package assembly, board assembly and testing. A major weakness of this approach is that it was not possible to evaluate the thermal performance of a new product or package until the first prototypes were available late in the design process. At this stage, there was only time to test one design alternative without delaying the product introduction. Between 80% and 90% of the time the product met thermal performance requirements and the product launch proceeded as planned.

However, 10% to 20% of the time, the initial package did not meet the requirements. In this case, mechanical engineers had to scramble to develop a new packaging option that met the thermal performance requirements. As a result, the product launch was typically delayed for six weeks in addition to the expenses involved in making design changes and re-running the physical tests. It took so long to evaluate each design that there was insufficient time to try alternative approaches in an effort to optimize thermal performance.

Thermal modeling provides fast results

For the past several years, IDT has developed a new process that substantially reduces the amount of time required to evaluate the thermal performance of new products. The new process takes advantage of the detailed, two-resistor and Delphi modeling methods that make it possible to quickly produce a computationally efficient representation of a component's thermal

characteristics. IDT engineers model the proposed design by going to Mentor Graphics' FloTHERM.PACK website and entering parameters to describe the IC package such as package type and size, lead or ball count, substrate cross-section, die size etc.

FloTHERM.PACK supports three types of package models – detailed, two-resistor and DELPHI. Detailed package models describe the package features in full and hence require significantly more computation resources as compared to two-resistor or DELPHI models and are the most accurate in thermal performance calculations. Two-resistor compact models are generated using computational implementation of the JEDEC standards for the Junction-to-Case and Junction-to-Board resistances. They offer an almost insignificant computational cost, and predict junction temperatures accurate to within 30% in the worst case. DELPHI compact models are an implementation of the methodology proposed by Project DELPHI, and are a significant improvement over two resistor models. In just about any reasonable electronics cooling environment at the system level, a DELPHI compact model will predict the junction temperature to an accuracy of 10% while greatly reducing simulation time.

The website generates a thermal model of the package that IDT engineers insert into a JEDEC standard environment that they have defined in FloTHERM thermal simulation software. The model is then solved quickly. The simulation results provide a complete understanding of the thermal performance of the design. They include not only the temperature difference between ambient and the junction but also the temperature of every point within the system.

“The simulation results help us identify areas with high thermal resistances that offer opportunities for improving thermal performance,” Shah said. “We can simulate a design alternative in only one day in the early stages of the design process so we have the opportunity to evaluate many different designs to optimize thermal performance. In many cases the simulation also provides insights that help us to improve the performance of the product.

For example, we can easily see whether or not a heat spreader is needed to meet the thermal requirements of the application.”

Simulation helps optimize design

Shah provided the example of a recent product launch in which simulation enabled him to evaluate several alternatives to optimize the design from a thermal perspective prior to the prototype phase. This product is a multichip module in a Micro Leadframe package that contains two dice, a processor and a clock. The thermal requirements of this application were particularly challenging because the temperature difference between the two chips needs to be maintained at 0.1°C or less. This is because the temperature affects the frequency at which the chips operate and these two chips need to operate at nearly the exact same temperature.

Shah considered two main design alternatives. Positioning the dice side by side on a die paddle has the advantage of providing a low thermal resistance between the two dice along with lower assembly costs and the disadvantage of taking up additional board real-estate. On the other hand, stacking the dice on top of each other takes up less board real-estate but normally involves higher thermal resistance and higher assembly costs. Shah created a series of thermal models to compare these two basic configurations using different die-to-die attach and die-to-paddle attach thermal interface materials.

For each design alternative, he entered the dimensions and material properties of the package into the FloTHERM.PACK web form. Then he downloaded the resulting model and imported it into the FloTHERM environment. He looked at a half dozen design alternatives over ambient conditions ranging from -55°C to 85°C. While the temperature of the dice had to be held below specified values, the primary challenge was holding the temperature difference between the dice to a very low level.

Saving board real-estate

“I had assumed that a side-to-side arrangement would provide the best thermal performance since the two dice are thermally connected through the die paddle and the die attach materials which could be used in that configuration were significantly more conductive than the stacked-die option,” Shah said. “But I discovered after running the simulation that the stacked die actually provided better performance. Looking more closely at the simulation results, I determined that the more efficient thermal interface material that could be used with the stack die approach outweighed the expected benefits of the side-to-side approach. The product is designed to be used in board-real-estate-sensitive hand-held consumer devices so the ability to use the more space-efficient stacked die approach provided a significant advantage to original equipment manufacturers.”

“This application is just one of many examples of how thermal simulation can improve the product development process,” Shah concluded. “Thermal simulation helps us increase revenues by avoiding late stage design changes that would otherwise delay product launches. Thermal simulation also reduces our product development expenses by reducing the need for physical testing and helping us avoid late-stage design changes. Finally, thermal simulation helps us evaluate design alternatives from a thermal standpoint and in some cases even enables us to deliver superior products timely to the market.”



Figure 1: IDT BGA package.

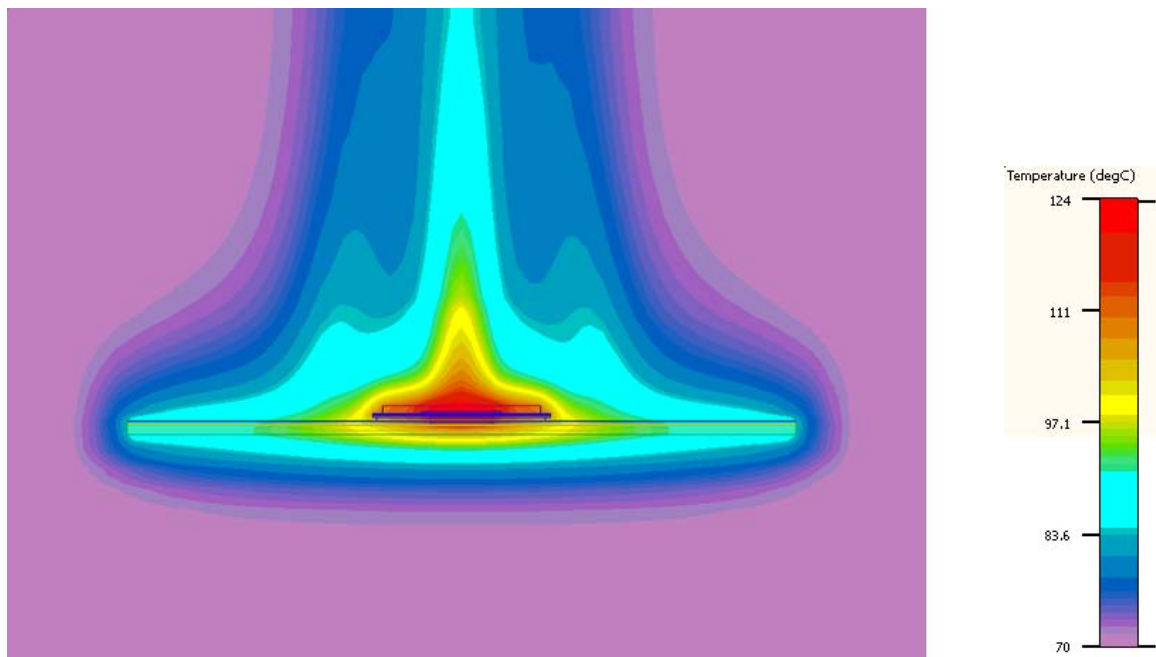


Figure 2: Plastic Ball Grid Array Package with 1oz copper planes in package substrate and no heat slug. Device Power = 3.5 W, Max. Die Temp allowed = 125 C, Max. Ambient Temp = 70 C. Thermal simulation result show that temperature is too close to maximum.

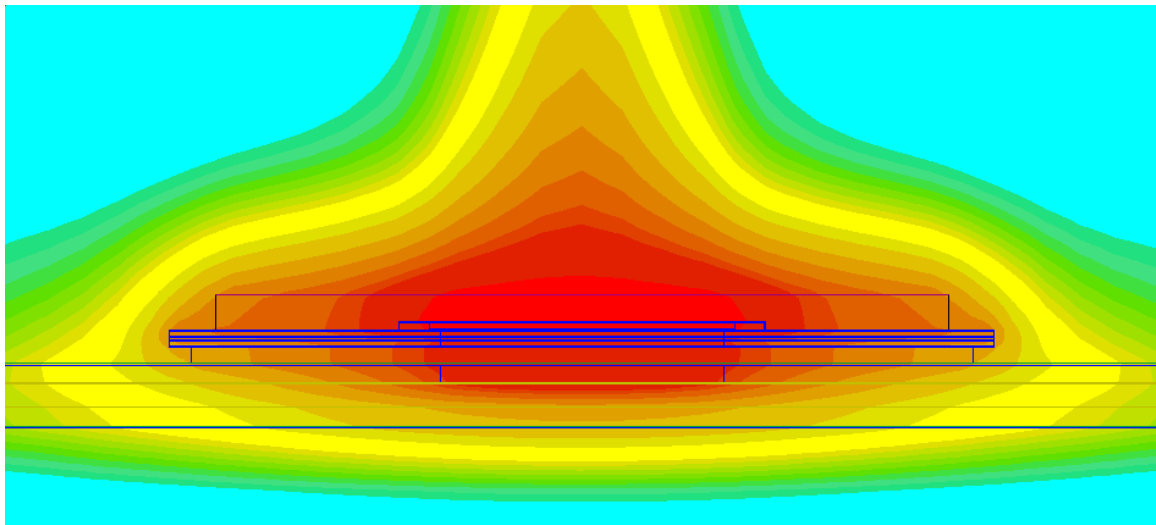


Figure 3: Zoomed-in view of Figure 2.

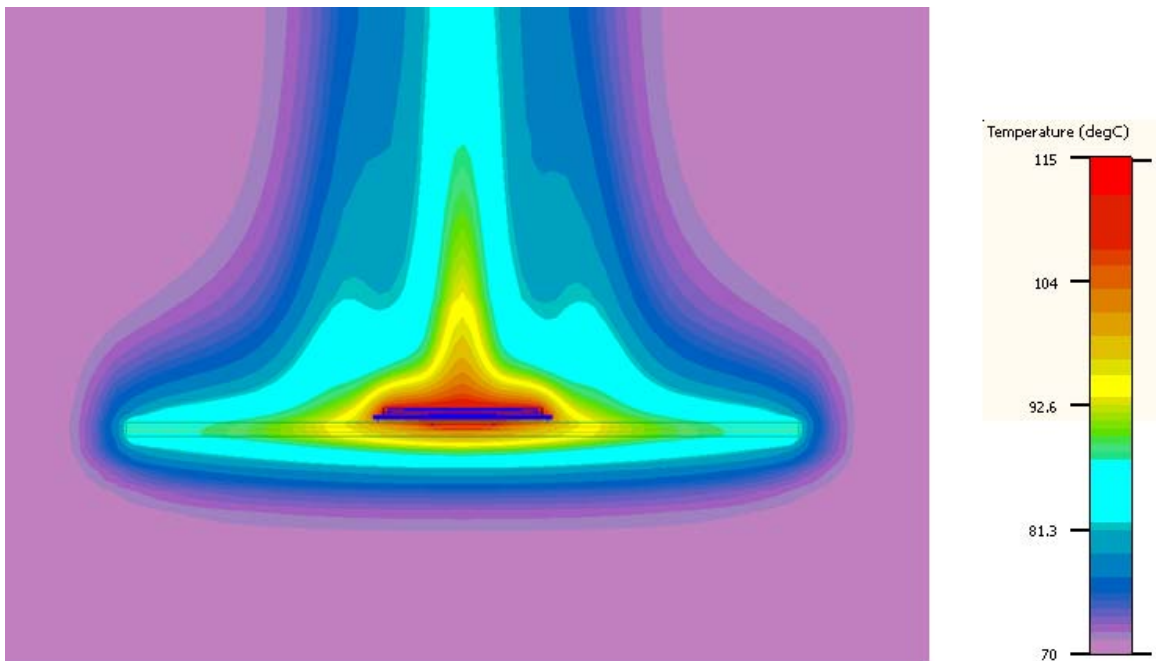


Figure 4: Same example as Figures 2 and 3 except that 2 oz. copper planes in package substrate and heat slug are used. The temperatures are now well under maximum levels but the 2 oz. copper planes and heat slug add cost.

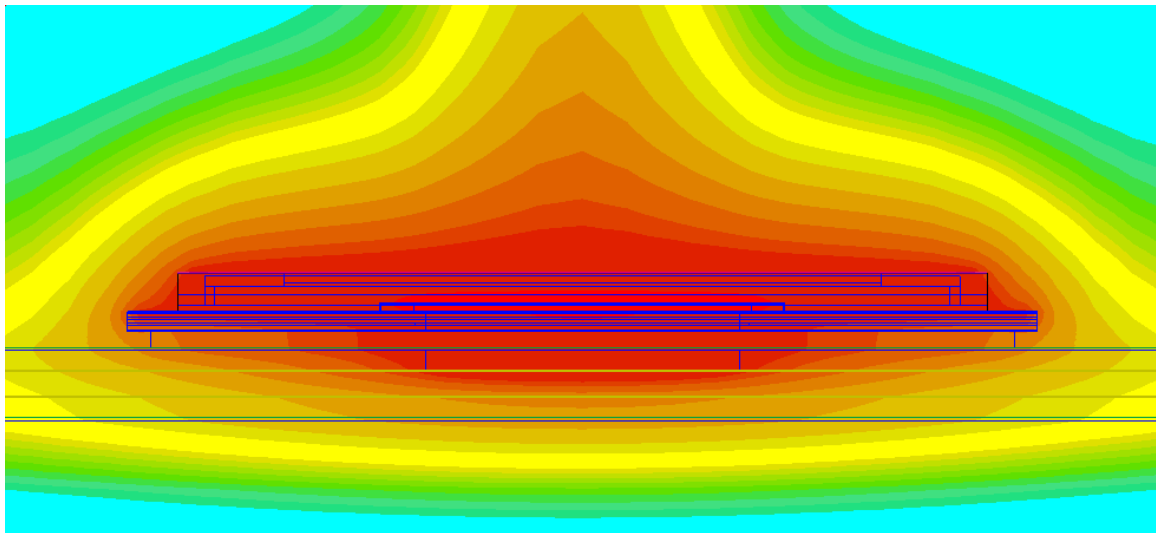


Figure 5: Zoomed-in view of Figure 4.

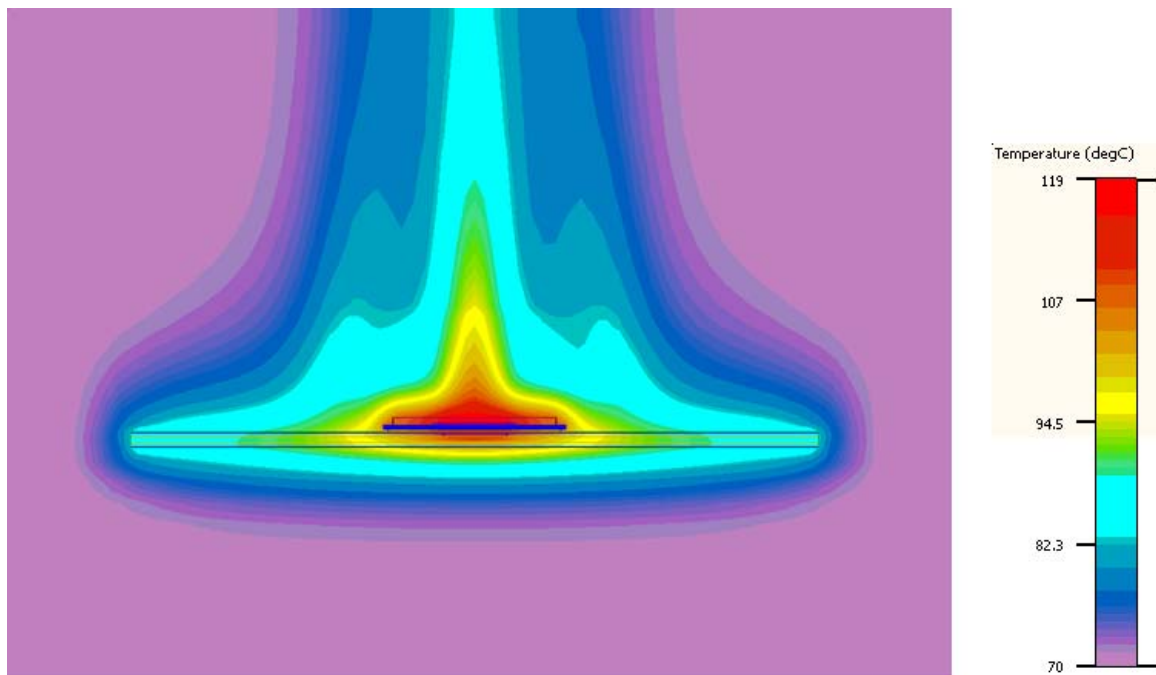


Figure 6: This design iteration uses 2 oz. copper planes and no heat slug. The cost is only slightly higher than the design shown in Figure 2 yet the temperatures have been reduced to acceptable levels. This was the final design.

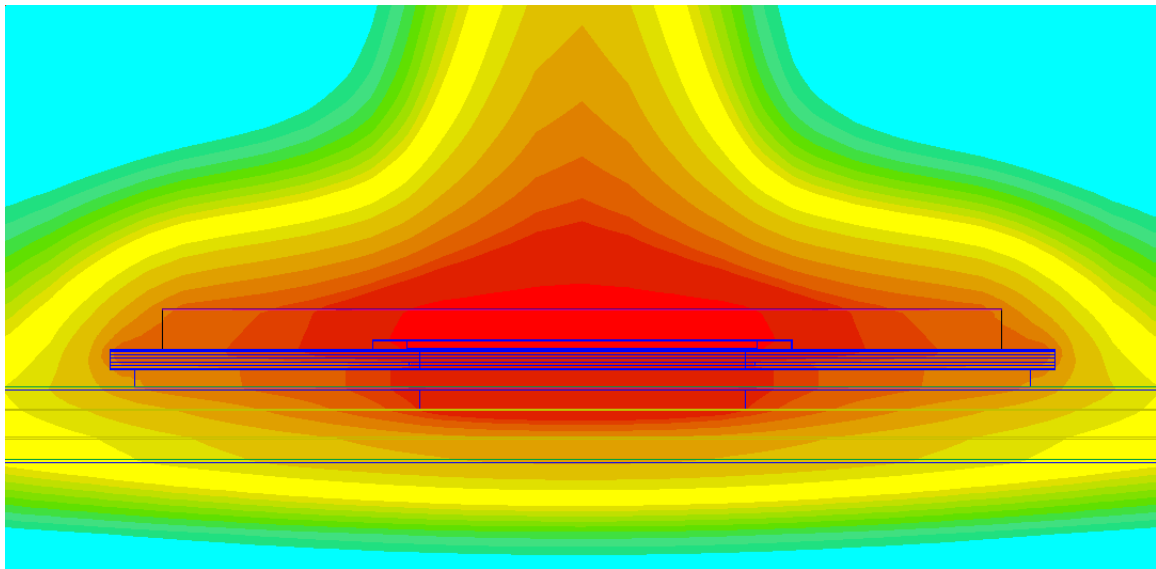


Figure 7: Zoomed-in view of Figure 6.

For more information about FloTHERM, visit

www.mentor.com/mechanical

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