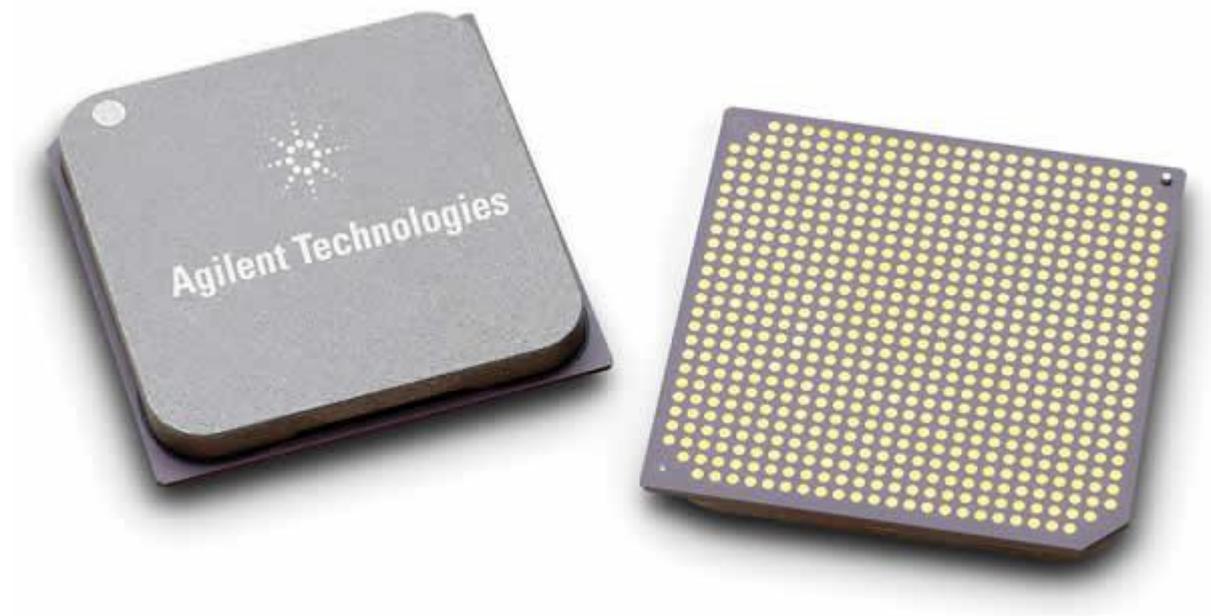


## Agilent Speeds Thermal Design for its Customers by Providing Compact Models

Agilent Technologies is simplifying and speeding up the thermal design process for its customers by providing compact models that can be used to predict the performance of its semiconductor solutions for networking in realistic electronics cooling environments.

Agilent has long used thermal simulation tools to produce detailed models that reconstruct the physical geometry of the package and accurately predict the temperature of the various elements within the package for a variety of conditions. More recently, the company has found it can save a considerable amount of time by using Flotherm's new Internet-based process for developing behavioral compact models that predict the temperature of the package at critical points such as the junction, case and board. "We can produce accurate, validated compact models of our new components in a matter of minutes," said Scott Burton, Package Analysis Engineer, for Agilent's ASIC Product Division, Fort Collins, Colorado. "The result is that we can generate simulated thermal characterization data based on JEDEC standard tests in much less time than was required with previous approaches. As an added feature, we can now provide our customers with models that they can drop into a full thermal design simulation. This allows them to model the behavior of the component in their system environment with minimal effort."

For over two decades, Agilent has designed and manufactured complex, high performance ASICs for applications including networking, computing, and imaging. Agilent offers state-of-the-art hierarchical design methodology and design-for-test capability and has an outstanding track record of first-pass success in the design and manufacture of these chips. These strengths, combined with an extensive IP portfolio, facilitate rapid integration of quality, high-performance ASICs.



### Need to supply thermal design information

Burton said that thermal information is required for most of the company's products. That's because it's useful for customers to have access to thermal characterization data based on standard tests such as EIA/JEDEC standard JESD51-6: "Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)."

This standard specifies the environmental conditions for determining thermal performance of an integrated circuit device in a forced convection environment when mounted on a standard test board. The thermal resistance measured using this standard is RJMA or QJMA, a forced convection environment with a specified air velocity and inlet temperature. In the past, the majority of

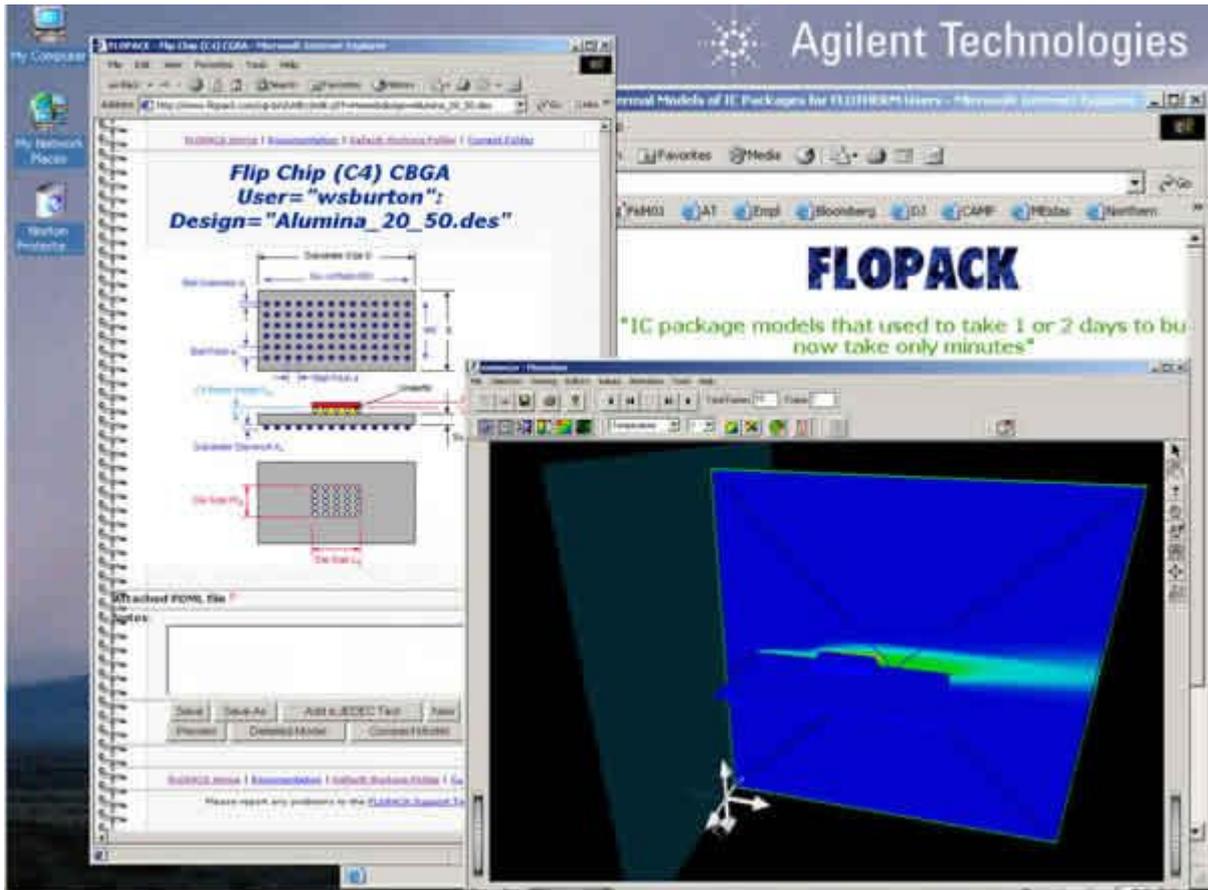
Agilent's networking and computing ASICs were supplied to customers that were involved in the design process from start to finish and those customers had complete access to component design information and decisions. This close relationship in many cases eliminated the need to provide standardized thermal design information. However, Agilent is now addressing a much broader group of customers and needs to provide thermal design information in a more universal format.

Agilent engineers have long used simulation software like Flotherm from Flomerics, for system- and component-level thermal analysis. At Agilent's ASIC Product Division, detailed package models are used to generate simulated standard thermal characteristics and the thermal design information needed by customers integrating Agilent components into their systems. "Creating this design information has its difficulties," Burton said. "Detailed models can often be difficult for customers to use because the 'conduction only' software models cannot be easily integrated into computational fluid dynamics (CFD) system simulations and even when they can, the complexity of detailed models can often computationally overwhelm system simulations. Distilling information from these detailed models into something simple and useful for customers can create its own problems," Burton continued. "Simple resistor models are not universally useful since each customer may need this information tailored to their own system and boundary condition information," Burton concluded.

So, Agilent took a close look at work done by the Delphi consortium, a publicly funded research project consisting primarily of electronics manufacturers and including one software vendor, Flomerics, that led to the first thorough methodology for the generation of boundary-condition-independent compact models. Boundary-condition-independent means that the models will predict the temperature of the various elements within the package accurately regardless of the computational environment in which it is placed. A compact model is not constructed to mimic the geometry and material properties of the actual component, but rather is an abstraction of the response of the component to various boundary conditions, such as flows, temperatures and pressures. It is important to note that the Delphi methodology is a non-proprietary, open methodology that is under active consideration by the JEDEC JC 15.1 committee on thermal phenomena as the framework for an industry-wide standard on compact modeling.

### **Creating Compact models on the Web**

"Flomerics has introduced a very easy and simple method of creating either detailed or Delphi models from what they call JEDEC Library Wizards," Burton said. "One can simply select the appropriate JEDEC package outline from a dropdown list, input the power and the die size and occasionally a few additional pieces of information for certain package sizes. The Web site then generates a compact or detailed thermal model of the component."



The JEDEC library wizard on Flomerics' [Flopac website](#) contains built-in common industry manufacturing and design rules used by most IC component suppliers. These results will generate package models from a reduced set of input parameters. A detailed Flotherm study that correlated Delphi models to physical testing results showed that it yields less than 10 percent error for the wide range of environments that were examined, including single bare package in natural convection, single package with heatsink in natural convection, single bare package in forced convection at two meters per second, single bare package under impingement flow with a jet velocity of one meter per second and package with neighboring components at forced convection at two meters per second. In each case a 4-layer (2S2P-two signal, two power plane) PCB with a size of 100 mm by 100 mm was used. The ambient temperature was +30C for the natural convection environments and +25C for the forced convection environments. Implementing Flopack as a Web application makes it possible to implement new package models or update older ones by simply changing a single copy of code on a central Web server. Flopack supports all major package styles, sockets, PCBs and heatsinks. Further validation of Flopack models is ongoing at Flomerics.

"When we create a new product, whether it is designed for the general market or a single customer, we always start with a detailed model," Burton said. "We're developing a process to validate these models by importing them into Flotherm and adding them to a model of the board that we use for electrical testing. The validated models are then added to a model of the board specified in EAI/JEDEC standard EAI/JESD51-3. The boards specified in this standard have very specific requirements for stock material, board outline and trace design. Using a model of the board that we have previously validated with physical testing and a validated compact model of the component makes it possible to accurately simulate standard tests that determine parameters such as the junction-to-top-center of the package and junction-to-board that we provide to customers on a data sheet. This eliminates the expense and lead time that would otherwise be required to build JEDEC standard boards, assemble the component and perform a series of physical tests."

"The value of creating a compact model goes far beyond the ability to create data sheets more quickly and inexpensively," Burton continued. "If all we provided to our customers was data

sheets, in many cases they would come back to us with questions such as: 'how did you obtain this particular number?' or 'can I use this number in my application environment?'. For Agilent customers that use Flotherm for system thermal simulation, we can now simply provide them with the boundary condition independent compact model that they can insert into their system model to evaluate the thermal performance of the component under any conditions they want to observe. This saves the time required to create a component model and allows them to obtain information under any conditions they want as opposed to the limited information provided by the JEDEC standard tests."

"While the compact models that we create are specific to Flotherm, a large part of the industry use them, including all Agilent customers, so up to now there has been no compatibility or data translation issues," said Burton. "Finally, another advantage of this approach is that by providing nearly every significant piece of thermal information, the need to share sensitive IC design information, in most cases, is eliminated."