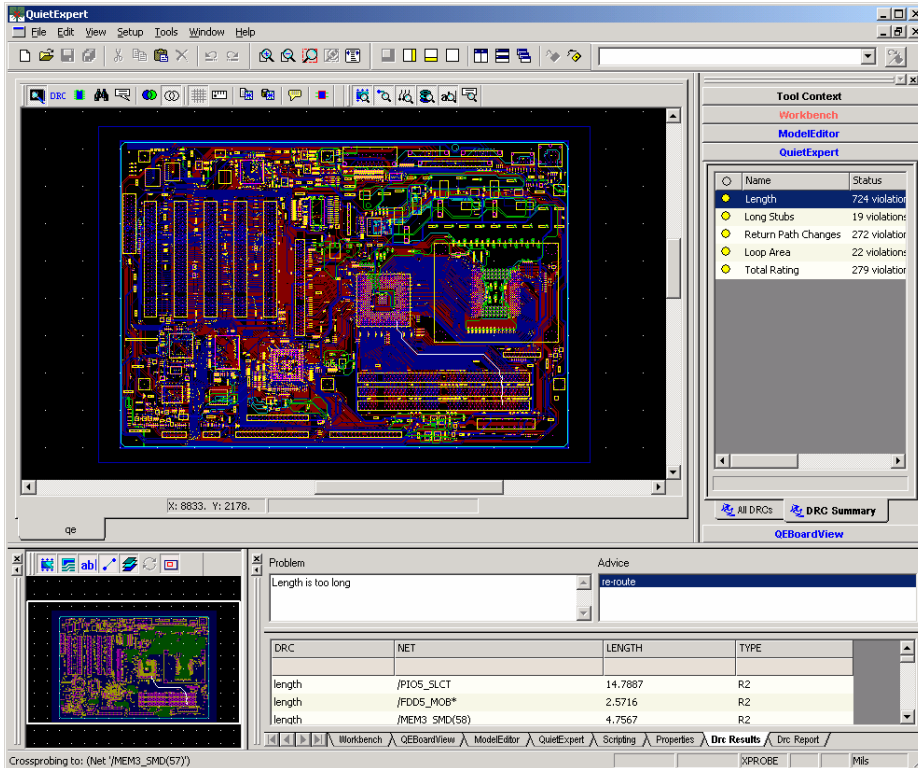


Quiet Expert



Quiet Expert: An integrated environment for easily spotting EMC problem areas on a PCB design

Major product features:

- Complete EMC analysis tool for PCB layouts
- Scans design and flags areas of potential EMC problems
- Provides quantitative analysis on predicted EMI levels using algorithms pioneered at the University of Missouri, Rolla
- Advice on fixing potential problems aids in creating correct design to meet strict EMI regulations
- Full integration into most major layout tool flows
- Powerful DRC rule API allows for implementation of complex DRC rules for both EMI and signal integrity

A Complete EMC Methodology

Quiet Expert provides board designers and layout engineers with a powerful way to check their PCBs for incorrect or dangerous routing structures that may cause EMI problems. The tool will not only locate the problems by highlighting them in the integrated board viewer, but also report the cause of the problem and advice on possible solutions. It can be used throughout the design cycle, even on a partially routed board so the design teams can have immediate feedback on the layout before it is complete. The ease of use model allows for all teams in the design phase to benefit from the technology. This method of analyzing the board early in the design cycle is the single, most cost-

effective way to analyze boards for potential EMI problems.

EMC Based Design Rule Checker

At the heart of the Quiet Expert analysis is the advanced design rule checker (DRC). The DRC analysis uses both physical and electrical parameters to verify the design and determine problem areas. The combination of using both allows the tools to provide a comprehensive EMC based analysis. A powerful API enables creation of complex design rule checks which can include altering physical based rules parameters according to frequency. This is powerful in cases where higher frequency nets must be routed according to stricter guidelines than

slower or less critical nets. Rules can also be parameterized, facilitating adjustment based on design type or product line.

Quiet Expert also includes built-in algorithms to predict radiation for any given net. These algorithms were pioneered by the University of Missouri, Rolla and provided to the UMR EMC Consortium, one of the biggest consortiums focused on EMC analysis in the U.S. The results produced in this analysis allow the designers to compare relative EMC levels predicted from different nets on the board so violating nets can be prioritized.

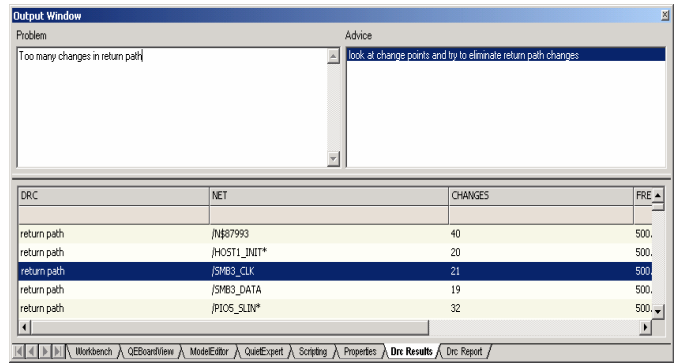
Easy Viewing of Results

Results are easily viewed in several different ways. They are output in a spreadsheet-like window that conveniently displays all pertinent information of any particular DRC. These results can be sorted to any parameter, including net name and type of violations on that net. This facilitates finding areas of concern quickly and easily. Alongside the results are messages for problem and advice for that particular net. The messages can be customizable by the user, and can even be programmed for any international language.

These results are also automatically cross probed to the integrated board viewer so the user can immediately see where the problem exists on the board. Several highlighting options are available to the user to specifically emphasize the violating area. In addition, the viewer contains full layer display control to assist in examining the exact structure in question.

Customizable Flow control

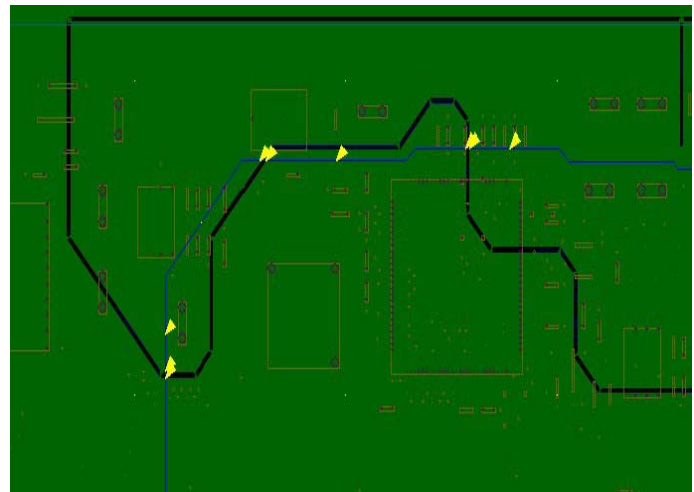
A customizable flow control provides



The screenshot shows a software window titled "Output Window" with a "Problem" pane and an "Advice" pane. The "Problem" pane contains the text "Too many changes in return path". The "Advice" pane contains the text "look at change points and try to eliminate return path changes". Below the panes is a table with columns for DRC, NET, CHANGES, and FRE. The table lists several return path violations for nets like /M87993, /HOST1_INIT*, /SMB3_CLK, /SMB3_DATA, and /PIOS_SLDV*.

DRC	NET	CHANGES	FRE
return path	/M87993	40	500.
return path	/HOST1_INIT*	20	500.
return path	/SMB3_CLK	21	500
return path	/SMB3_DATA	19	500.
return path	/PIOS_SLDV*	32	500.

Full reporting on all results include description of problem, advice on how to correct it, and parameters pertinent to the analysis of each net.



Complete highlighting of potential problems is supported. Here, a clock net crossing multiple gaps is shown with markers signifying impedance changes on the net.

the flexibility to adjust to any corporate design flow. The result is a fully automated transition into the software, making it powerful yet easy to use. Proprietary tasks such as reading in different modeling formats, linking into schematic capture tools, or using databases managed by PDM systems are all possible with the use of the flow control.

It also allows supports automatic notification of analysis complete and database packing which supports the team based approach to PCB layout and analysis.

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