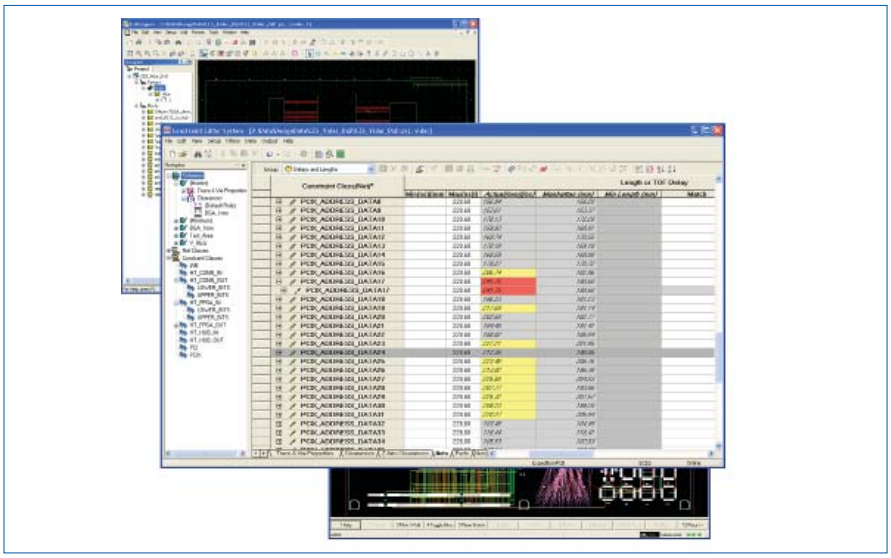
Constraint Editor System

System Design

Reduce Costs and Accelerate Time-to-Market

D A T A S H E E T



CES spreadsheets integrated to schematic and layout environments.

MAJOR BENEFITS:

- Single, integrated constraint entry and edit tool for design, layout, analysis, and manufacturing rules.
- Powerful and easy-to-use spreadsheet-like GUI guided by the design database and cross probing to applications.
- Hierarchical constraint entry speeds input of complex rules on many objects.
- Speeds time-to-market with informal and formal constraint reuse, concurrent constraint entry, and editing.
- Improves design productivity with extensions allowing in-tool constraint editing.

Introduction

As PCBs increase in complexity and density, a higher percentage of the design must be implemented with strict adherence to design rules. Manual documentation, translation, and interpretation of design rules often cause longer product development cycles and increased costs. The Constraint Editor System (CES) provides a fully integrated, constraint-driven design methodology that reduces design costs and time-to-market by automating design rules communication and eliminating unnecessary PCB prototypes and re-spins. CES provides both electrical engineers and PCB designers with direct control over the most advanced routing technology in AutoActive to solve current and future system design requirements.

Constraint Integration throughout the Design Flow

CES supports bi-directional cross probing, highlighting and selection between a spreadsheet-based constraint interface, and schematic capture and physical design tools in the flow. Constraint values are fully synchronized during the forward and backward annotation processes with intelligent handling of connectivity changes. CES also supports importing constraint templates developed with HyperLynx LineSim®.

Concurrent Design

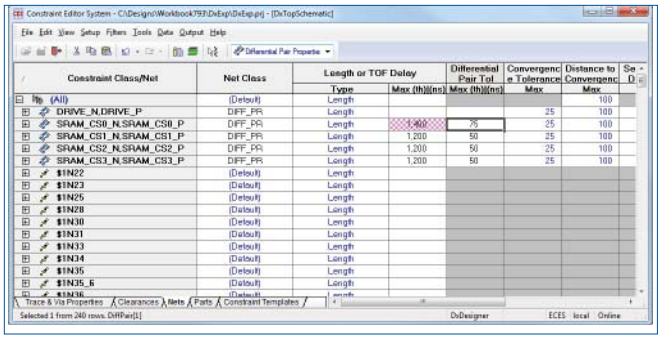
Increased complexity puts more pressure on design teams to get things done on time. CES allows many designers to work on the constraint data at the same time. The CES database architecture was designed to allow multiple edits simultaneously. This eliminates overhead of manual techniques that other systems must use. CES provides locking mechanisms to prevent concurrent users from editing the same data, and it also provides notification of who is changing which data to the team. This means projects schedules can be met by applying more resources to a project.

Constraint Reuse

CES allows reuse of many of the simple and complex rules that have been created. Constraint templates can be used to copy constraints from one net to another net or an entire bus, including custom ordering, net constraints, and pin pair constraints. These templates can be used on other designs as well. CES also supports Reusable Blocks, allowing designers to use an entire circuit, constraints, and physical layout data from one design into another design. Reusing constraints saves time and improves quality by allowing the designer to use a previously completed and verified circuit instead of creating a new one.

Hierarchical Rule Classes

With CES, users can create hierarchical rule classes that greatly ease the association of constraints to design ob–jects. With more common "flat" systems, users must apply constraints to many individual nets or pins, but with the use of hierarchy, and the inheritance of constraints that this facilitates, those same nets can be constrained by one rule at the class level. This greatly reduces the number of constraints manually entered in the design; when changes occur, due to packaging or other requirement changes, constraint modification is simple and straightforward.



Graphical notification of concurrent edits.

Topology Assignment

CES supports user-defined and pre-defined automatic topologies. Users can create a topology and associated constraints with virtual pins or they can use the more sophisticated automatic topologies where the AutoActive® environment intelligently manages virtual pin locations.

Net Class Schemes

Schemes allow users to have area-specific manufacturing constraints, which override the design-wide or layer-specific constraints. These include constraints such as widths and clearances, which may have to be modified, for example, around a Ball Grid Array device. These schemes are then mapped to rule areas in the AutoActive environment.

Differential Pair Creation

Differential pairs have become more and more prevalent in designs. CES allows users to easily assign these with a differ–ential pair finder utility. This utility allows users to assign differential pairs using common naming conventions, wild card searches on net names, and information from interactive selection of pairs of nets across the entire design.

Impedance Planning

Users can view or modify the stackup properties associated with a design within CES. By doing so, users can verify existing stackup characteristics, such as differential pair impedance, modify layer attributes, and/or augment the stackup to meet width, spacing, and impedance constraints. This is the same stackup editor and field solver used in the popular, industry-leading Signal Integrity Analysis tool suite, HyperLynx.

Parallelism/Crosstalk Rule Assignment

CES provides a simple parallelism rule creation and assignment dialog box. Parallelism rules apply on the same or adjacent layers and can be assigned at the net or class level for maximum control and flexibility. Alternatively, users may provide constraints on a crosstalk basis; that is, using electrical specification of the rules as well as physical (parallelism) rules.

System Requirements

Operating Systems:

- Red Hat Enterprise Linux: WS 4
- SuSE Linux Enterprise 10
- Solaris: 10
- Windows: XP Pro, Vista (32 & 64 bit), 7, Server 2003/2008

Memory:

- 512 MB Minimum; 2 GB Recommended

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