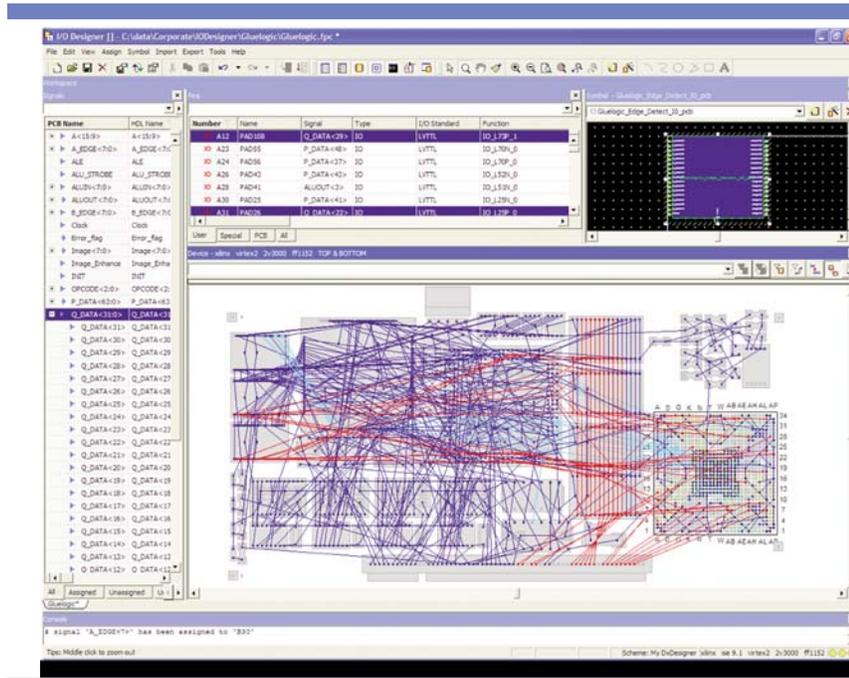


# I/O Designer for FPGA

Optimize the FPGA/PCB Co-Design Process

FPGA-on-Board Design

D A T A S H E E T



## Major product benefits

- Enable an FPGA/PCB Co-Design process
- Up-to-date FPGA vendor device support
- Correct-by-construction I/O assignment
- Fast and easy PCB symbol and schematic creation
- I/O optimization and pin swapping in the PCB design process
- I/O optimization based on actual PCB layout component orientation
- I/O optimization to partial traces for BGA breakout and escape paths

## Overview

FPGAs are widely used in many industries and applications. But, every FPGA must ultimately reside on a PCB. Historically a manual process or numerous scripts were utilized to incorporate the FPGA into the PCB design. This process was satisfactory for smaller and less sophisticated devices, but, today's FPGAs are powerful devices with high pin counts, numerous I/O standards, and high speed capabilities. The new generation of FPGAs has pushed the manual process to its breaking point. The result is longer design times and less than optimal FPGA-to-PCB interface design.

Intelligent design of the FPGA interface is a requirement to leverage FPGA devices to meet leading edge system interface requirements such as DDR3. Repeatedly achieving a high interface design standard requires an effective FPGA/PCB co-design process. An effective co-design process not only shortens your time to market, but provides the optimal FPGA-on-Board implementation, which lowers costs and improves overall quality. FPGA usage is so ubiquitous that the benefits of an effective FPGA/PCB co-design process will be realized essentially on every PCB design.

Mentor Graphics offers I/O Designer, the foundation for an effective FPGA/PCB co-design process. I/O Designer supports the latest devices offered by the FPGA vendors and can quickly convert an FPGA design into a PCB schematic, ready for layout. In addition, I/O Designer provides correct-by-construction FPGA I/O assignment, allowing pin swapping and layout-based I/O optimization within the PCB process.

## FPGA Support

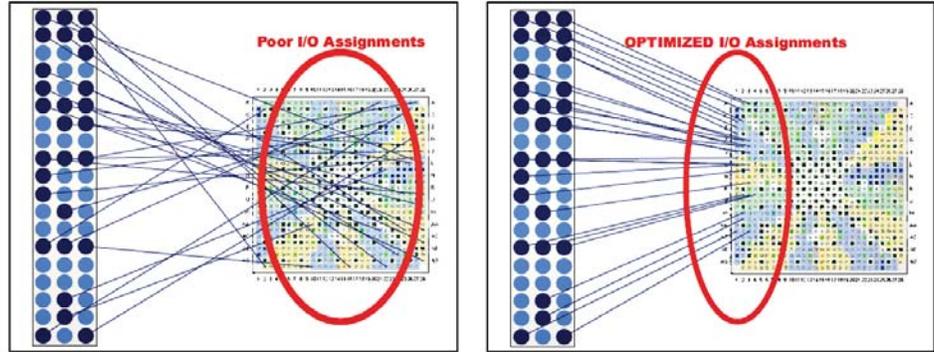
I/O Designer provides support for the latest FPGA devices through strong partnership collaboration with the leading FPGA vendors. I/O designer fully supports the following industry leading FPGA vendors: Actel, Altera, Lattice, and Xilinx. FPGA vendor's native file formats are supported for bi-directional exchange of device and pin assignment

information. In addition, I/O Designer has built-in I/O assignment rules that are specific to each device so pin assignments can be easily made within the tool. This capability brings pin assignment rules to the PCB domain, enabling pin swapping and I/O optimization based on actual layout data. Pin assignment rules within the PCB domain is a requirement for any effective FPGA/PCB co-design implementation.

## Symbol and Schematic Generation

Once the initial signal assignment is complete, the next step is to create or import the symbol set for the FPGA. The user has the option to use a generic symbol or symbol set directly from the corporate library or create a custom symbol or symbol set for a specific FPGA design. For custom symbol usage, I/O Designer can create the functional block and symbol set based on a variety fracturing parameters. If generic symbols are preferred, I/O Designer can import them directly from the corporate library.

I/O Designer then exports the symbols to the schematic and automatically makes the pin connections based on the signal/pin assignment. This process can save days or even weeks of work. Typically the pin assignments will change multiple times during the design process for a number of reasons including but not limited to PCB routing congestion, FPGA timing and PCB timing. When pin changes do occur, I/O Designer can do a quick update to the schematic in seconds, saving even more time.



Optimize I/O assignments to improve PCB quality and lower costs.

## Pin Swapping and I/O Optimization

The most powerful capability of I/O Designer is optimizing the I/O assignment to reduce the number of layers, shorten traces, and reduce the number of vias. I/O Designer offers two ways to optimize pin assignments: pin swap and layout based optimization. I/O Designer enables classic layout pin swapping by adding swap rules to the component. The user can then easily swap pins in the context of the PCB layout tool. With layout based optimization, I/O Designer uses the actual PCB layout to reassign pins based on component location and connectivity. Once I/O Designer loads the PCB layout, the user is free to use manual or automated techniques to optimize to pins or partial traces for BGA breakout and escape paths. This powerful capability lowers PCB costs and improves signal integrity, producing a higher quality PCB.

## System Requirements

- Windows 7 x86/x64
- Windows Server 2008 x86/x64
- Windows Server2003 x86/x64
- Windows Vista x86/x64
- Windows XP x86
- Linux RHEL 4 x86 and Linux RHEL 4 x86-64
- Linux RHEL 5 x86 and Linux RHEL 5 x86-64
- Linux SLES 10 x86-64
- Solaris 10 UltraSPARC

To learn more, call Mentor Graphics or visit our web site at [www.mentor.com/pcb](http://www.mentor.com/pcb).

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