

Meeting the Challenges of DDRx Design

Q&A from the Live Presentation

DDRx Simulation Questions

- Q. How long does it take to run the simulation described in this seminar?
- A. Simulations can take 2 to 3 hours to run for a full DDRx interface if you simulate every net on the Address and Data buses.
- Q. When using DDR2 ODT, is series termination still required? If not, are there any advantages to having discrete series termination?
- A. No, series termination is not required. Because of the flexibility in drive strength and different ODT settings, there is no significant advantage in having discrete series termination. This will generally add unnecessary components to your board.
- Q. Does HyperLynx support a hybrid simulation for DDR3 (eg, IBIS models for drivers and receivers and Spice models for the transmission lines)?
- A. Yes. HyperLynx has a built-in 2D Boundary Element Method (BEM) field solver that provides modeling for transmission lines. Because these are modeled as W-element lossy transmission line models, there is no need to have a separate SPICE model for the transmission lines.

In addition, the HyperLynx DDRx wizard supports a hybrid IBIS simulation for driver/receivers and SPICE passive elements such as package models and connector models.

- Q. Should eye diagram analysis be used for DDR3?
- A. Eye diagram analysis could be used, but it isn't necessary. Eye diagrams are generally used for multi-Gigabit serial technologies where there is an embedded clock signal and you're measuring eye aperture and jitter against a bit error rate requirement.

With an eye diagram, you may over-design because the best you can do is measure from your worst-case clock edge to your worst-case input threshold for setup or hold. In reality, those edges may not be associated with each other so you may see a timing failure that doesn't actually exist.

That's not the case for DDR signals – this is a source-synchronous interface. Instead, you want to measure edge-to-edge timing from clock to address, data to strobe, and strobe to clock. All of these measurements can be made without an eye diagram and, since HyperLynx makes these measurements on every valid edge, you know exactly what your timing margins are.

- Q. Is address termination required for DDR3 if a DIMM is not being used (i.e. a single DDR3 chip)?
- A. You need to run simulations to determine this. In some cases, you can overdrive the circuit if you don't use this pull-up termination. I have seen designs run reliably without termination but the work was done upfront to validate that it would work.
- Q. Can DDR batch simulations be run on an embedded DDR2/3 design?
- A. Yes, the wizard can be used for embedded DDR2/3 designs. Just select Slot 1 and Rank 1 (if it's a single-rank system) in the wizard and the results would be valid.
- Q. How good are the simulation results compared to measurements?
- A. As long as you have good IBIS models for the drivers and receivers, HyperLynx results are very good and reliable compared to physical measurements. For examples of DDR2 correlation, view the following application note from Altera:
http://www.altera.com/literature/hb/external-memory/emi_plan_board.pdf.

- Q. What are the typical electrical problems seen for DDR3?
- A. Data signals generally look fairly clean. The issues usually arise on the address bus where there is heavy loading. The fly-by architecture helps, but it's still not perfect signal quality.
- Q. The tool reports SI failures for non-monotonocities and multi-threshold crossings; if data/address have adequate setup/hold margin results, does it matter?
- A. If the setup and hold times are met, then the non-monotonocities are generally not a problem. This does, however, reduce the overall margin in your design and should be avoided if possible. One thing to watch for with non-monotonocities or multi-threshold crossings is the impact that crosstalk might have on reducing your margin.
- Q. Are the simulations based on schematic or layout? If they're based on layout, do you run ElectroMagnetic field simulation?
- A. The simulations could be run either way; in a pre-layout schematic format in HyperLynx LineSim, or with the actual layout in HyperLynx BoardSim. Both HyperLynx tools use a 2D Boundary Element Method (BEM) field solver to extract the electromagnetic behavior of the trace geometries, so yes, it is an electromagnetic field solution.
- Q. Does the simulation consider skew and SI issues due to board layout? Is HyperLynx able to add these parameters to the simulation?
- A. Yes, if you are simulating in HyperLynx BoardSim, the skew from routing and the SI issues from terminations, vias, impedance changes between layers, etc. are accounted for automatically in your simulation.
- Q. What kind of data are in the spreadsheet; you went through it quickly?
- A. There are several different spreadsheets that are generated by the wizard.

First, there is a spreadsheet that contains all the signal quality measurements – items like overshoot, non-monotonic edges, etc.

Second, there are spreadsheets generated with the timing information on the interface. These are separated into different spreadsheets for the Address bus, Data bus, and Strobe to Clock skew measurements. These are then broken down into an All Cases report, a Worst Case measurement report, and a Failure Report. This gives you access to all the information and also filters out some data for you.

In the timing spreadsheets, we provide information on read/write operation, driver/receiver, time in the clock or strobe signal where the measurement was taken, the required setup/hold time, the adjusted setup/hold time based on input slew rate, final setup/hold time, and setup/hold margin.

- Q. I'd like to look at the example that you used to simulate. Can you post it on your website?
- A. At this moment it's not widely available to everyone, but it can be delivered on request. Email me, Steven.McKinney@mentor.com, if you'd like a copy of it.
- Q. Does the simulation take into consideration the effects of DDRx signals crossing different voltage/GND planes?
- A. No, it does not consider this effect. This would result in crosstalk in the return path of the signals and reduce your voltage and timing margins, so it is generally considered a very bad design practice, especially for DDR3 speeds. This can also result in EMI issues.

Model Questions

Q. Are SPICE models appropriate for this type of simulation?

A. SPICE models are not required to accurately model the behavior of the driver/receiver. The main limitations of IBIS are with modeling pre-emphasis and equalization, which is why the IBIS AMI standard evolved.

Since DDR2 and DDR3 do not use this technology, a standard IBIS model is sufficient. The one area where SPICE may be valuable is in modeling the package of the controller since the internal package lengths can be long. I have seen IC vendors provide SPICE package models for their controllers, but an IBIS Package file will also be accurate enough for the speeds of most of these interfaces. Because the package is generally small on the DRAMs, using lumped RLC information in the standard IBIS model is generally appropriate for the DRAMs.

Q. Do you need any information other than Altera's IBIS model for Altera devices?

A. Yes, to do an accurate timing analysis you also need to have some timing information about the controller. The main pieces of information you need are the following:

- Address/Command valid before Clock rising edge (tCKAC)
- Control valid before Clock rising edge (tCKCTL)
- DQS rising edge with respect to Clock rising edge (tCKDQS)
- DQ/DM transition window before DQS transitions (tDQSDQ)
- DQ setup and hold window relative to DQS transitions (tDS, tDH)

Q. Do module manufacturers supply models for their modules?

A. Yes, generally the module vendors will supply models for their modules. Typically they are provided as EBD models but you also can get the actual routing of the DIMM modules. For DDR3, these are controlled by the JEDEC specification and all DIMM vendors have the same routing. For DDR2, routing is generally the same across DIMM vendors but there is no JEDEC specification, only tolerances for the routing on each card type and what the topologies should look like.

Q. What if you don't have IBIS models and only have SPICE models? Can these be imported?

A. SPICE models cannot be used to simulate I/O behavior; you need to use IBIS. However, you can use SPICE for the passive parts of the interconnect, parts like packages, connectors, etc.

Questions about the DDRx Wizard

Q. Can you use the wizard on RLDRAM2 or DDR2 SRAM, or is it specific to SDRAM applications?

A. This is specific to SDRAM. If the timing relationships between RLDRAM2 / DDR2 SRAM and SDRAM are similar, theoretically you could use the wizard to do the timing analysis but we would need to experiment with it to see whether the behavior is correct.

Q. I use LPDDR2, does the wizard support that?

A. The HyperLynx 8.1 version of the wizard will support LPDDR and LPDDR2. Currently in beta testing, HyperLynx 8.1 is expected to be released in Q1 2010.

Q. Is there a document on the DDR wizard?

A. Mentor customers with access to SupportNet, can view several AppNotes on the setup of the DDRx wizard and on the review of spreadsheet results. Also on SupportNet is a detailed video on the DDRx wizard that walks through all the pages in the wizard.

- Q. Do you have wizards for PCI-Express, SATA, etc.?
- A. We currently do not but Mentor is investigating support of additional wizards for commonly used technologies. We do offer design kits for these technologies which are available on the Mentor SupportNet site.

License & System Questions

- Q. What PCB file formats are supported when importing board information to HyperLynx?
- A. HyperLynx supports all the mainstream CAD environments. Mentor BoardStation, PADS, Expedition; Cadence Allegro; Zuken CADSTAR and CR-5000.
- Q. What kind of PC and memory does HyperLynx require?
- A. There are no specific hardware requirements but I would generally recommend at least 1GB of RAM and a 2+GHz processor to get decent performance.
- Q. What version of HyperLynx supports DDR analysis?
- A. In HyperLynx 7.7, we added support for DDR2 slew-rate derating measurements using the HyperLynx Oscilloscope. HyperLynx 8.0 includes everything in HyperLynx 7.7 as well as all the DDRx wizard capabilities that were shown in this session.
- Q. What version of HyperLynx do I need for this simulation?
- A. You need to have HyperLynx 8.0.

Other Questions

- Q. Can you tell us more about write leveling and what it is?
- A. Write leveling is essentially a type of dynamic timing on the controller. When a controller is writing to multiple DRAMs, write leveling gives the controller the ability to delay the output of the DQS and DQ/DM signals relative to the clock for each byte lane.

This is necessary because the Address and Clock signals use a fly-by architecture which means that the Address and Clock are in a daisy chain going from DRAM to DRAM. But the DQS and DQ signals are not daisy chained, they go straight to the DRAMs. This creates a timing skew at some DRAMs between when the clock arrives at the DRAM and when the DQS signal arrives. Because there is a clock-to-strobe timing relationship that has to be maintained, it's necessary for the controller to be able to delay the launch of the DQS and DQ signals by the amount of interconnect delay between the DRAMs. This delay in the launch of the DQS and DQ will align the time between when these signals arrive at the DRAM and when the clock arrives at the DRAM.

- Q. Is there a place in the presentation where write leveling is talked about?
- A. Yes - Slide 8 discusses write leveling.
- Q. Can a read follow a write in a single cycle?
- A. The read and write transactions are handled separately in the analysis.
- Q. Where can I learn more about DDRx?
- A. Current customers can visit SupportNet, <http://supportnet.mentor.com/reference/technotes/public/technote.cfm?tn=MG250320>, for design examples and a list of DDRx resources that will help you understand DDRx design challenges, prepare for simulation, set up and run simulations, and analyze simulation results. Other interested readers should contact a Mentor sales person or local distributor.

Archived webcast available from:

<http://www.mentor.com/products/pcb-system-design/multimedia/ddrx-design-webinar>

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