

Optimizing Power Delivery with Effective Decoupling

Q&A from the Live Presentation

HyperLynx® PI

Power Integrity Basics

- Q. Can you give a brief explanation of spreading inductance?
- A. Briefly, spreading inductance is caused by current going from a narrow pin or via and spreading out through the plane.
- Q. How do you determine what kind of capacitors value?
- A. This is a good question. Typically you need a range of values: larger caps to provide low impedances at lower frequencies, and large numbers of smaller, low-inductance caps to provide low impedance at higher frequencies.
- Q. Is there a rule on impedance requirement?
- A. The target impedance for a PDN is "very low." This is discussed in the presentation.
- Q. How can I determine if my design needs PI simulations?
- A. Good question. Typical design characteristics that mandate PI analysis are: partitioned / segmented planes, high current requirements, inability to follow manufacturer decoupling guidelines, and desire to reduce cost.
- Q. This may be an SI question. Do traces better reference to a ground plane at top and its split power planes at bottom, or two ground planes at top and bottom?
- A. That is an SI question, but I will answer it. :-) Actually, it does have some implications for PI as well. The simplest answer is that you should maintain a solid reference throughout. So if you reference ground and transition to another layer, that other trace should also reference ground. And there should be a stitching via next to the transition via to allow for the AC return current to jump from one ground plane to the other.
- Q. Is there a rule of thumb for how much bulk capacitance should be added to the PDN based on the expected load?
- A. The bulk capacitance of the Power Distribution Network (PDN) is determined by the impedance requirement. However, typically one large electrolytic cap meets most impedance requirements for the low frequencies.
- Q. Are the vias in pad models different than outside the pads?
- A. Yes, via-in-pad mounting tends to give lower mounted inductance than regular via mounting. This is discussed in a paper on our website about the "Power Integrity Effects of HDI," <http://www.mentor.com/products/pcb-system-design/techpubs/download?id=47102>.
- Q. Do we need IC modeling when doing PI?
- A. For DC Drop, you do need to model the IC as a current sink.
- Q. Is there any reason why people should keep the power planes in the middle?
- A. Power planes are most effective when placed closest to the caps. However, this is just one trade-off in designing a stackup. HyperLynx PI allows you to quantify the trade-off of putting planes in the middle versus on top or bottom.
- Q. When you say "solid planes," what does that mean? We often have shared power planes with more than one voltage on them.
- A. Solid planes just means not made up of traces or hatched. Shared power planes are of course simulated (in fact, they are one of the main reasons a PI analysis tool is necessary).

Power Integrity Basics (cont.)

- Q. When designing double-sided boards, you often don't have the luxury of decoupling at the pins of large BGA devices. Is there a rule of thumb on decoupling planes vs. local decoupling in terms of picking capacitor values?
- A. The values are picked based upon what is necessary to maintain low impedance across a wide frequency range (typically a value per decade). Planes are effective at higher frequencies and, depending on their configuration, can help eliminate a number of the smaller value caps (0.01uF and maybe 0.1uF, for example).
- Q. Do the decoupling caps on the PCB side cause resonance at lower or higher frequencies when looking at the full PCB+package+chip system?
- A. Lower frequencies, when compared to on-chip decoupling. The packaging and pin parasitics (mainly inductance) isolate the chip from the board so that the board is only effective up to ~ 1 GHz.
- Q. Does a typical IBIS model include power draw characteristics, characteristics that can be used in PI analysis?
- A. No. IBIS does not yet have the infrastructure to allow for PI modeling.
- Q. When using ferrite beads, is it useful to split up analog and digital supply planes to Chip?
- A. This is an often-debated topic. Basically it ends up being a trade-off between trying to isolate noise versus starving a chip for power (and thus creating more local noise).
- Q. How can you measure the high-frequency impedance and high-frequency inductance of a PDN?
- A. This is what decoupling analysis does. In the lab, this can be measured with a VNA.
- Q. I have heard about theories and reports that discourage use of various size decoupling caps in a design because of their intercap loop noise created by their varied time constants.
- A. This is interesting. I guess I would have to see the paper to assess the validity of the claim, but I have not heard much about this. I think most people would agree (both through simulation and measurement) that using a number of different cap values is the most effective method of putting together a low-impedance PDN.

HyperLynx PI Capabilities

- Q. Does HyperLynx recommend and identify where to place the decoupling caps?
- A. Yes. You can determine this using what-if analysis in LineSim.
- Q. Are there any technologies that are not recognized, ie., layer specifics, odd layer stackups etc...?
- A. The only special requirement of AC analysis is that you have solid planes. By solid planes, I mean not hatched or made up of traces. Partial/split planes are, of course, supported.
- Q. Will HyperLynx PI also highlight the Hot spots?
- A. Yes. This will be discussed in the DC Drop webinar, <http://www.mentor.com/products/pcb-system-design/events/dc-drop-analysis-webinar>.
NOTE: After Dec. 16, 2009, view the *archived* webcast, <http://www.mentor.com/products/pcb-system-design/multimedia/dc-drop-analysis-webinar>.
- Q. Can HyperLynx address the use of multiple values of parallel caps at a given location? For example, 10uF + .1uF + 10pF?
- A. Yes, absolutely. That is one of the things that makes HyperLynx PI so useful.

HyperLynx PI Capabilities (cont.)

- Q. Can HyperLynx predict any magnetic coupling due to high current switching noise found near the switching node of PWM regulator circuits?
- A. Interesting question. That depends on the coupling mechanism. If you are referring to coupling through the PDN then, yes, it is included.
- Q. Can we include ferrite beads to stitch planes together?
- A. Yes, ferrite beads can be included in the analysis.
- Q. Can we include particular power planes and not include the whole board?
- A. Power analysis can be performed on one rail at a time. If you want to view the effects of only a few planes for a given voltage rail, you can do so with the what-if capabilities in LineSim.
- Q. Can HyperLynx compute the impedance of a termination resistor with frequency including the termination supply model?
- A. Yes.
- Q. Can simulation cover both self-generated and external coupled noise?
- A. Yes.
- Q. Does HyperLynx simulate split-plane effects?
- A. If the problem is in relation to PI analysis, then yes. If by split planes you mean split reference planes with reference to SI or EMC analysis, no. I would suggest: a) not using split planes as reference planes, or b) taking a look at QUIET Expert., <http://www.mentor.com/products/pcb-system-design/circuit-simulation/quiet-expert/>.

HyperLynx PI How-to Questions

- Q. How does one view the overall mounting inductance that the tools calculate? Does HyperLynx distinguish mounting inductance and the caps' inherent ESL? I tend to ignore the latter since the mounting inductance dominates.
- A. Good question. Mounting inductance can be viewed by itself after doing a "quick analysis" in the decoupling wizard. ESL and mounting inductance can be entered separately, and are distinguished in the tool.
- Q. Only a few vendors provide models in HL format. Any plans to get more vendors involved?
- A. The format for cap models is actually universal. S-parameters, SPICE models, and simple RLC models can all be used in HyperLynx.
- Q. Does the model include coupling through vias transitioning through planes?
- A. Yes, this is one of the most important parts of the model, and is included.
- Q. How does one enter the information about the capacitors? Can we input models based on part number or does one have to enter a model and manually associate it with each part being simulated?
- A. Capacitor models are applied in groups of like capacitors, and groups are assigned by default. You can assign models to individual capacitors or groups, and groups can be re-grouped as desired.
- Q. What kind of capacitor models are used in HyperLynx, time variant? Can they be customized?
- A. S-parameters, SPICE models, and simple RLC models can all be used in HyperLynx. And yes, they can be customized.

HyperLynx PI How-to Questions (cont.)

- Q. Does HyperLynx have models for "Low Inductance" capacitors (ex. 4 terminal caps)?
A. These caps can be modeled.
- Q. How does HyperLynx calculate the mounting parasitics? Or do we have to model it outside of HyperLynx?
A. HyperLynx calculates the mounting parasitics from the board layout data.
- Q. One of the problems I encountered playing with HyperLynx is in modeling the noise source properly so that the tool will get me an accurate result, specifically in modeling my DDR2 interface noise environment. Will the tool offer some suggested models to use for the source, so that my results will be realistic?
A. Most customers have luck getting rail-draw info directly from their IC manufacturer, or from on-board measurements.
- Q. In doing PI, does HyperLynx count the power source as an ideal model or does it count all disturbances from the power source?
A. You can use simple or complex models for VRMs.
- Q. Can HyperLynx analysis be used to determine value/placement of bulk capacitance?
A. Yes.
- Q. Can you specify the shape (dimensions) of a power shape in LineSim?
A. Yes.
- Q. If I overlay 2 "round" vias to create a pseudo "oblong" vias on the board, can that be analyzed?
A. There isn't such a thing as oblong vias - I think you mean antipads. If so, yes that will work.
- Q. How does HyperLynx handle/understand voltage sense line? Can it be included as part of VRM model?
A. This is actually more of a DC Drop issue, and will be discussed in the DC webinar, <http://www.mentor.com/products/pcb-system-design/events/dc-drop-analysis-webinar>, on December 16. Hope to see you there!
- Q. Does the tool handle multi-board or board + package situations?
A. It only simulates one board at a time. Actually I am not sure it would be very valuable or practical to simulate multi-board situations since the associated connector/package inductances effectively isolate the two board power domains such that it makes more sense to simulate them one at a time.
- Q. Do you have any comments about having the power plane at top and bottom and the signal plane in the middle?
A. Power planes are most effective when placed closest to the caps. However, this is just one trade-off in designing a stackup. HyperLynx PI allows you to quantify the trade-off of putting planes in the middle versus on top or bottom.
- Q. In LineSim do you specify the shapes of the power distribution copper (as well as the stack up)?
A. Yes.

HyperLynx PI How-to Questions (cont.)

- Q. How does HyperLynx estimate the constantly changing, switching loads of a processor / FPGA? i.e., the processor clock speed may not change, but the processing load "frequency" may change unpredictably.
- A. PDN Analysis looks at the PDN itself. The phenomena you describe would relate to calculating the "target impedance" for the PDN analysis (to which you compare the results). You should use the worst-case condition to calculate your target impedance.

Accuracy of HyperLynx PI

- Q. Are there any case studies showing an actual product measurement vs. simulation? Something like trying to model up a BGA in LineSim before any cad data is really available?
- A. Yes. See the correlation paper entitled done by Dr. Eric Bogatin on our website. The paper is called "Establishing Confidence in PDN Simulation," <http://www.mentor.com/products/pcb-system-design/techpubs/download?id=47080>,
- Q. Doctor Bogatin refers to it in his paper verifying accuracy of HyperLynx PI - it is used to eliminate measurement and probing artifacts.
- A. Dr. Bogatin's paper about the accuracy of HyperLynx PI is on our website. See "Establishing Confidence in PDN Simulation," <http://www.mentor.com/products/pcb-system-design/techpubs/download?id=47080>.
- Q. Is there an instrument that would verify by measurement the simulation of the high frequency impedance of a PDN?
- A. In the paper from Eric Bogatin, <http://www.mentor.com/products/pcb-system-design/techpubs/download?id=47080>, he uses a VNA to compare simulated and measured results.
- Q. I have built capacitors using spice, s-parameters, and simple models and simulated and tested them using the PI tool - very good agreement.
- A. Thanks!

Slide-specific Questions

- Q. It appears you generated Z11 plot for the Z profile - why not Z21 for example?
- A. Z11 is the impedance of the PDN at that location - which is really what we are after.
- Q. Thanks for the overview. I would suggest you explain HOW to use HyperLynx PI to perform the various calculations (how to find the right cap values and numbers) rather than just stating the tool can do it.
- A. Good suggestion. Note that demos are also available online, <http://www.mentor.com/products/pcb-system-design/multimedia/filters/hyperlynx-c3befda1-tag/product-demo-type>, and from your local AE.
- Q. For noise analysis, how do we model package and IC parasitics?
- A. Noise analysis is performed at the board level. The noise source used in the analysis is what appears at the power pin of the IC.

Slide-specific Questions (cont.)

- Q. Are there any plans to be able to import IC outlines into LineSim? For instance, I have a BGA and would like to assign current sink models to the different pins. It would be nice to import the outline into LineSim and assign current sink models and simulate the PDN with reasonable estimated power planes. This might be a good add-on feature. It would help predict ahead of time much better than a more simplistic VRM /current sink model.
- A. Good suggestion. Note that all power pins are brought into LineSim when doing an export from BoardSim.
- Q. Does the Z analysis compute and factor in the impedance/inductance of the power distribution copper shapes?
- A. Yes.
- Q. In the Ztarget calc example, you used the whole 5% in the calculation. Shouldn't you subtract the output tolerance of the power supply? Also, what about the output ripple of the power supply, shouldn't it be considered as well?
- A. Yes, that is a good point. For DC Drop, this is especially important.

Licensing & Support

- Q. Is HyperLynx PI a subset of the original HyperLynx?
- A. HyperLynx PI uses the same GUI, but can be purchased independently of HyperLynx SI.
- Q. Is DC Drop the only feature available in HyperLynx 8.0?
- A. DC Drop, AC Analysis, model extraction, and co-simulation, and a number of SI features are all available in HyperLynx 8.0.
- Q. What PCB file formats are supported?
- A. All major layout tools are supported in HyperLynx.
- Q. Is there a demo version of LineSim?
- A. We can set up an eval license for you if you are interested.
- Q. Are the AC analysis tools available in 8.0?
- A. Yes, they are available in LineSim.
- Q. Are there multiple versions of PI?
- A. There are a number of different PI bundles for different types of analysis, both DC and AC.
- Q. What about PI-SI-Timing co-simulation?
- A. This is another available option for customers who own HyperLynx SI.
- Q. The PI stuff is going to take additional licensing, correct?
- A. Correct. There are separate licenses for SI and PI analysis.
- Q. Has AC analysis been released for HyperLynx 8.0, or is it still in beta?
- A. AC Analysis is currently released in HyperLynx 8.0 in LineSim (what-if/pre-route). AC Analysis is currently in beta for BoardSim (post-route) and will release within the next couple months.
- Q. Is co-simulation a separate purchasable option or does it come with the DC or AC modules?
- A. It is separate.

Useful Links

VIDEO: Eric Bogatin discusses the importance of power integrity analysis (6:15 mins),
<http://www.mentor.com/products/pcb-system-design/multimedia/player/bogatin-enterprises-customer-reference-0cc12cf4-c5a3-4827-8b94-c3e92ce3914b>

PRODUCT DEMO: Decoupling Analysis (3:25 mins),
<http://www.mentor.com/products/pcb-system-design/multimedia/overview/hyperlynx-pi-decoupling-analysis-demo-52ed7a4b-3a43-4622-8206-c37ca31c5aa4>

PRODUCT DEMO: DC Drop Analysis (2:45 mins),
<http://www.mentor.com/products/pcb-system-design/multimedia/overview/dc-drop-analysis-with-hyperlynx-pi-1f906b0b-d134-4d94-b6b6-b69ff38d8770>

TECHNICAL PAPER: Power Integrity Effects of HDI,
<http://www.mentor.com/products/pcb-system-design/techpubs/download?id=47102>

TECHNICAL PAPER: Establishing Confidence in PDN Simulation,
<http://www.mentor.com/products/pcb-system-design/techpubs/download?id=47080>

WEBCAST: Optimizing Power Delivery with Effective Decoupling (24:26 mins),
<http://www.mentor.com/products/pcb-system-design/multimedia/optimizing-power-delivery-decoupling-webinar>

WEBCAST: Solving IR Drop Challenge for Effective Power Delivery (to be posted Dec. 17, 2009),
<http://www.mentor.com/products/pcb-system-design/multimedia/dc-drop-analysis-webinar>

WEBCAST OVERVIEW: HyperLynx 8.0 for Signal & Power Integrity (57:23 mins),
<http://www.mentor.com/products/pcb-system-design/multimedia/power-integrity-hyperlynx>

POWER INTEGRITY WEBPAGE: Power Integrity webpage,
<http://www.mentor.com/products/pcb-system-design/circuit-simulation/hyperlynx-power-integrity/>