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BGA Breakouts & Routing

Effective Design for Very Large BGAs

Excerpt from Chapter One

The Problem

The increasing pin-count and decreasing pin-pitch of BGAs amplifies already difficult design problems. Maintaining signal integrity at high performance levels and reducing fabrication costs are arguably the two most important requirements. Unfortunately, these requirements are conflicting. Reducing crosstalk is generally accomplished by increasing the space between conductors which can increase layer count. Plus, routing dense BGA packages require smaller design rules and more layers. Smaller features and increasing layers contribute significantly to board cost. This is nothing new; yet further miniaturization of BGA packages will force us to deal with new thresholds of difficulty.

Many PCB designers who are using leading-edge high pin-count BGAs claim that the breakout of the device is the greatest contributor to the number of PCB layers.

Why have breakouts? Wouldn't it be better to route the device without breakouts? The answer is simple. If the BGA device has too many pins in a dense array, the only way to minimize the number of layers is to utilize all the available space inside the component area with a pattern of fanouts and breakout traces. Routing such a device without an effective pattern will certainly waste space and require more layers.

Not all BGAs present a routing challenge. Medium and low pin-count devices (less than 800 pins), even with a pin-pitch of less than .8mm, do not present a significant breakout problem and are usually routed without a breakout method. This means the pins are generally accessible and can be routed with a reasonable number of layers. The high pin-count devices (over 1500 pins) with a pin-pitch of 1mm or less require a strategy for getting the traces out of the array. Without a breakout strategy, the layer count will be excessive thus affecting the fabrication cost and reliability of the PCB.