TLA Design Entry Guidelines

Have you wondered why the design you submitted last year didn't make the cut? Your design could be the most complex on the planet, but the data you submit may not effectively distinguish it. This guide is intended to answer frequently asked questions and improve your entry. At the end of this document you'll find a sample of the complete entry form.

1. Upload design

This is an automated extractor that can simplify the data entry process and improve its quality. The extractor runs on your machine, and just pulls information to fill in the form (the database isn't copied). If you don't use the automatic extractor, use the design status/report functions in layout to find the required data then input it manually into the form. For details on the extractor, review the Automated TLA Extraction document.

2. Design category

The options for design category are shown below. Pick the one that most closely matches your end product.

- Consumer electronics & handheld
- Industrial control, instrumentation, security & medical
- Military & aerospace
- Computers, blade & servers, memory systems
- Telecom, network controllers, line cards
- Transportation & automotive

3. Tools used

Enter the primary design tools you used to create this design.

4. Advanced technologies

Check the box for all technologies you used in this design.

- RF/microwave
- Chip on board (wire bond)
- Buried capacitance
- HDI (high-density interconnect / microvias)
- Flex/rigid flex
- Flip chip
- Embedded passives

5. Design for …

If you had to work with constraints (on paper or in the system) for any of the following categories, check the box.

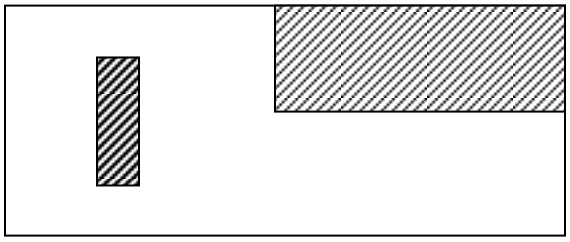
- Signal integrity
- Manufacturability
- Reliability
- Variants
- Power integrity
- Cost
- Govt. compliance

6. Units

Note that not all fields have the same unit: Imperial uses ‘in’ and ‘th’. Metric has ‘mm’ and ‘um’. Entering data off by 1000X is one of the most common errors. Note that existing data is not converted if you switch between Imperial and Metric – this must be done manually.

7. Board dimensions

The ‘usable area’ is basically the area within the board outline minus any significant cut-outs/voids (hatched in example below).



8. Layer stack-up

Specify the primary type (signal or plane) for each layer in the design. Also enter the total board thickness.

If you selected HDI as an advanced technology, you will be prompted to enter the number of HDI layers on the top and bottom sides. These are the additive, non-laminate layers only.

In the example below, there are 7 Total Metal Layers, 2 Top-Side HDI layers and 1 Bottom-Side HDI layer. Layers 3-6 are traditional laminate core.

9. Number of power/ground nets

Specify the number of unique supply nets (e.g. power rails) in your design.

10. Trace and via dimensions

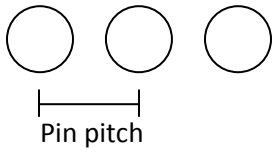
Enter the minimum dimensions used (e.g. for HDI sections or neck-downs into dense components). The typical (larger) dimensions are for average nets on the board.

11. Number of high-speed nets

Include any net with a high-speed constraint (e.g. length/delay, parallelism/crosstalk, matching/skew).

12. Smallest pin pitch

Smallest distance between high-density component pins, as measured below.



13. Fastest rise time

Fastest rising or falling edge time.

14. Placement (single/double-sided)

Specify whether you have components on just one or both sides of the board.

15. Number of active & passive components

Active: Components that require power to operate (e.g. power supply, fans, transistors, diodes, other ICs). **Passive:** Capacitors, resistors, inductors.

16. Total component area

This is the sum of component outlines including pads.

17. Comments

Write clear, concise descriptions of your design. This narrative will set your design apart from the otherwise bland numerical data. Don't assume that the numerical data speaks for itself! Highlight the "cool" stuff for us. Comments in this section are leveraged heavily in the judging.

For example, comments like "a lot of high speed nets" or even "73% high speed nets" does not impress the judges as much as a more detailed description of those net classes ("64 SERDES differential pairs matched to 25 thou") and a description of how you overcame the challenge of pre-analysis, routing, post verification and correction of those nets.

You may include a full product spec as an attachment, but please provide a summary of it in the Comments space.

a. Most complex component

   Describe what made it complex (e.g. tight pin pitch, number of pins, pin pattern, packaging, functionality).

b. Constraints

   List the types of constraints that were imposed on this design, based on the "Design for…" categories you selected (e.g. timing, noise, manufacturing). In addition, note other constraints like short design schedules, prototype limitations, product cost restrictions, etc. Give a few quantitative examples.

c. Design challenges

Talk about some of the business challenges you faced (e.g. time to market, product cost, development cost, functional differentiation, design cycle time). Discuss how these impacted the design team (e.g. round-the-clock designs due to time pressure; limited resources; extra prototype iterations due to performance goals or manufacturability issues; design partitioning; performance vs. manufacturing tradeoffs; RF circuit design/verification; minimizing noise in the power supply; design had to completely routed by hand). Give a few quantitative examples.

Talk about some of the advanced PCB fabrication technologies you had to use (e.g. first-time implementation of HDI/microvias; embedded passives; stacked die).

Think of images or documents that would illustrate these challenges (e.g. a screen shot of breakout patterns out of a complex BGA).

d. Innovative use of Mentor's design solutions

Talk about how you were able to overcome the challenges mentioned above. Discuss the role your design tools played in that effort (e.g. using XtremePCB to meet an aggressive schedule; I/O Designer to optimize system performance; PADS Layout to manually layout the entire board; automated custom applications; leveraged Expedition's BGA breakout algorithms).

18. Attachments

Upload images and/or documents that effectively illustrate the complexity of your design.

Do include:

- At least one full-board image and one close-up highlighting an interesting section of the layout. If you have a multi-layer board, don't turn on all layers in all your screen shots. The judges will be more impressed if they can distinguish details in your design rather than a shot that just shows a mash of interconnects. Capture the images with the layout tool in full-screen mode using the highest monitor resolution possible.
- An alternative to screenshots is a PDF output from the tool – these are high resolution, scalable, and show individual layers.
- Bonus points if you include individual-layer images of at least 25% of the total signal layers, and a photo of the manufactured board.
- Extra bonus points if you send a CCZ file of your design (see the Automated TLA Extraction document for details – see step #5). You may also supply the ODB++ output file prepared for manufacturing.
- Short documents that describe the products functional specifications.

Don't include:

- Your actual design database. The judges do not have the products needed to view these files (and you're probably exposing more IP than your management is comfortable with).

Tips for successful entries:

- Enter accurate numerical data for the design (all fields must be filled for submission to be accepted). Please review the sample completed forms below.
- Provide a minimum of 50-100 words per comment field.
- Include board images that clearly convey the complexity of the design (single-layer images are better than ones with all layers turned on).

Comments from the judges:

- "I advise all participants to thoroughly fill in all the blanks. Although we can determine many things about the design from your screen shots, a significant portion of the grade is based on the information you provide in writing. Mentor has gone to great lengths to give you an opportunity to get some of the recognition you deserve. So show us that you are more than a "hook up artist" and that your design truly deserves to be among the ones chosen for recognition. Good luck to you all."
  Pete Waddell President,
  UP Media Group
- "All judges for the Technology Leadership Awards (TLA) have previously designed printed circuits, so we appreciate your work. However, in order to accurately assess your submission, we need clear descriptions of the design challenges you faced (the WHAT) and your ultimate solution for these challenges (the HOW). Unless you tell us the specifics, we may not see the "genius" in how you faced your design challenge—regardless if it's simple or complex. I appreciate a good picture or illustration, so I encourage you to provide screen captures of layouts, simulations, stack-ups, etc."
  Happy Holden
  Senior Technologist, Mentor Graphics

If you have questions or problems with the data-upload program or design entry process, please contact David Wiens at pcb_tla@mentor.com or call +1 720.494.1086.

TLA Sample Entry Form

This section steps through the entry form for the TLA contest, showing sample values. After a successful submission, you will be mailed a PDF report of your entry.

2011 PCB Technology Leadership Awards - Disclaimer

By participating in the Technology Leadership Awards contest, you warrant that your Submission is your own original work, created solely by you and that you have the right to transfer all rights in it to Mentor Graphics Corporation. For the purposes of this contest, "Submission" shall mean the work provided to Mentor Graphics, such as textual and graphical descriptions of a product, and not the actual product.

By entering this contest you acknowledge and agree that Mentor Graphics Corporation, at its discretion, may publish any part of your Submission, including, but not limited to, screen shots and images of the design, your name and your company or school affiliation. Mentor Graphics Corporation may publish this information when disclosing winners, in press releases, on web sites, in presentations or in any other promotional publication.

Mentor Graphics Corporation is not responsible for any lost or misplaced submissions.

Technology Leadership Awards 2011

Accept Decline

If you have questions Technology Leadership Award or design entry process, please contact Dave Wiens at pcb_tla@mentor.com or call +1 720.494.1086.

Design Submission

1) Contact Info | 2) Overview | 3) Details | 4) Comments | 5) Attachments | 6) Confirmation

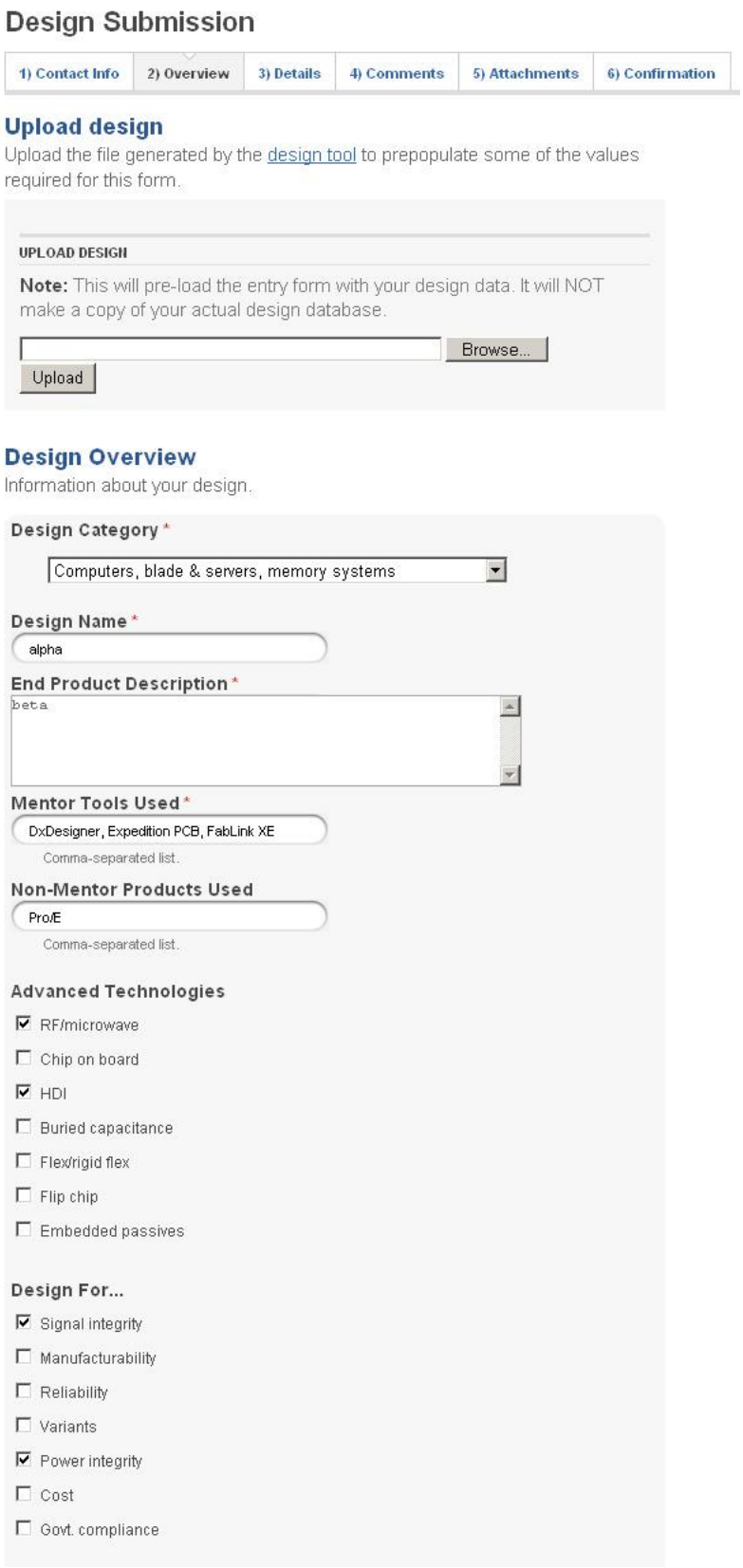
Contact Information

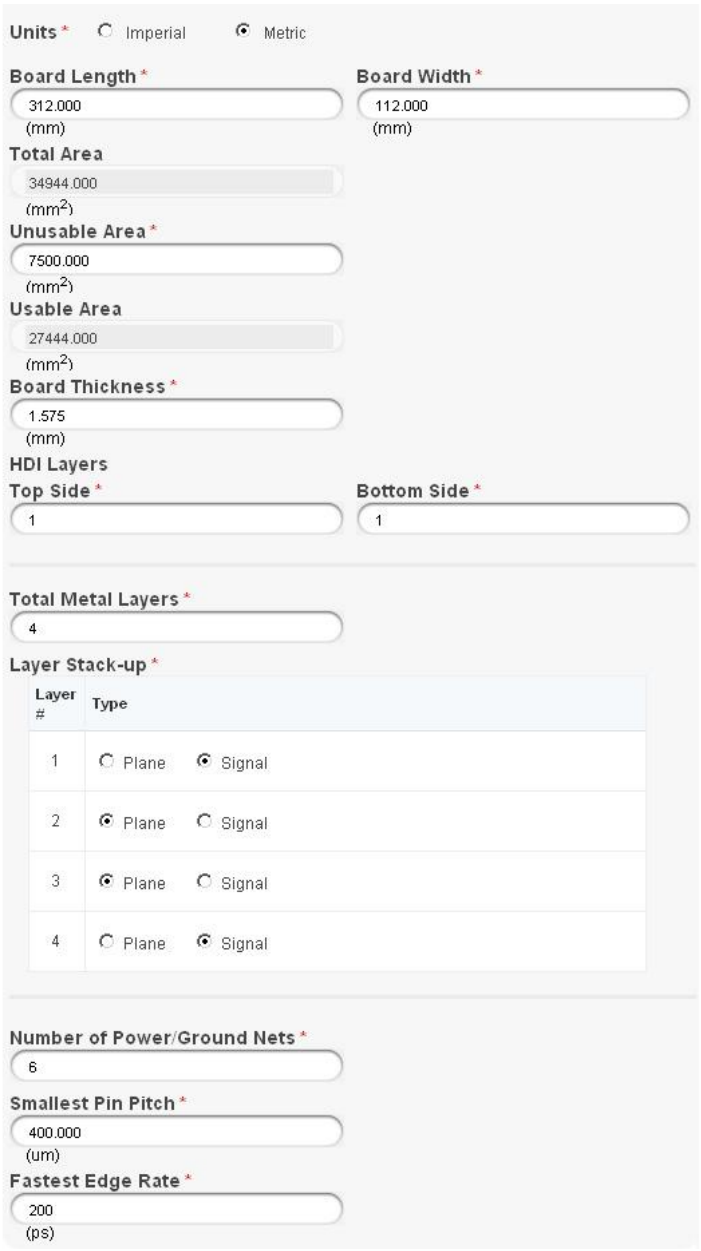
Please provide the following information about yourself.

First Name * John	Last Name * Smith
Email * john.smith@acme.com	Phone * 303-123-4567
Company * Acme Electronics	
Additional Designer Names	
Mentor Graphics Contact	
Street Address * 1811 Pike Road	
Address Line 2	
City * Longmont	State / Province / Region * CO
Postal / Zip Code * 80501	Country * United States

If you would like to be able to return to and edit your submission before it is completed, please enter a username and password.

Username jsmith	
Password •••••••	Verify Password •••••••


Design Submission
1) Contact Info
2) Overview
3) Details
4) Comments
5) Attachments
6) Confirmation
Upload design
Upload the file generated by the design tool to prepopulate some of the values required for this form.
UPLOAD DESIGN
Note: This will pre-load the entry form with your design data. It will NOT make a copy of your actual design database.
Browse...
Upload
Design Overview
Information about your design.
Design Category *
Computers, blade & servers, memory systems
Design Name *
alpha
End Product Description *
beta
Mentor Tools Used *
DxDesigner, Expedition PCB, FabLink XE
Comma-separated list.
Non-Mentor Products Used
Pro/E
Comma-separated list.
Advanced Technologies
RF/microwave
Chip on board
HDI
Buried capacitance
Flex/rigid flex
Flip chip
Embedded passives
Design For...
Signal integrity
Manufacturability
Reliability
Variants
Power integrity
Cost
Govt. compliance


Units * Imperial Metric
Board Length *
312.000
(mm)
Board Width *
112.000
(mm)
Total Area
34944.000
(mm2)
Unusable Area *
7500.000
(mm2)
Usable Area
27444.000
(mm2)
Board Thickness *
1.575
(mm)
HDI Layers
Top Side *
1
Bottom Side *
1
Total Metal Layers *
4
Layer Stack-up *
Layer #
Type
1 Plane Signal
2 Plane Signal
3 Plane Signal
4 Plane Signal
Number of Power/Ground Nets *
6
Smallest Pin Pitch *
400.000
(um)
Fastest Edge Rate *
200
(ps)

Design Submission

1) Contact Info | 2) Overview | 3) Details | 4) Comments | 5) Attachments | 6) Confirmation

Details

Please provide details of your design.

Trace Width/Spacing

Minimum Width * 63.500 (um)

Minimum Spacing * 76.200 (um)

Typical Width * 101.600 (um)

Typical Spacing * 101.600 (um)

Via/Pad Size

Minimum Hole Size * 127.000 (um)

Minimum Pad Size * 254.000 (um)

Typical Hole Size * 508.000 (um)

Typical Pad Size * 2032.000 (um)

Number of Vias * 12324

Number of Nets * 2314

Number of High-speed Nets * 463

Number of Pin-to-pin Connections * 13568

Total Trace Distance * 114650.000 (mm)

Placement * ○ Single-sided ◉ Double-sided

Number of Components * 3263

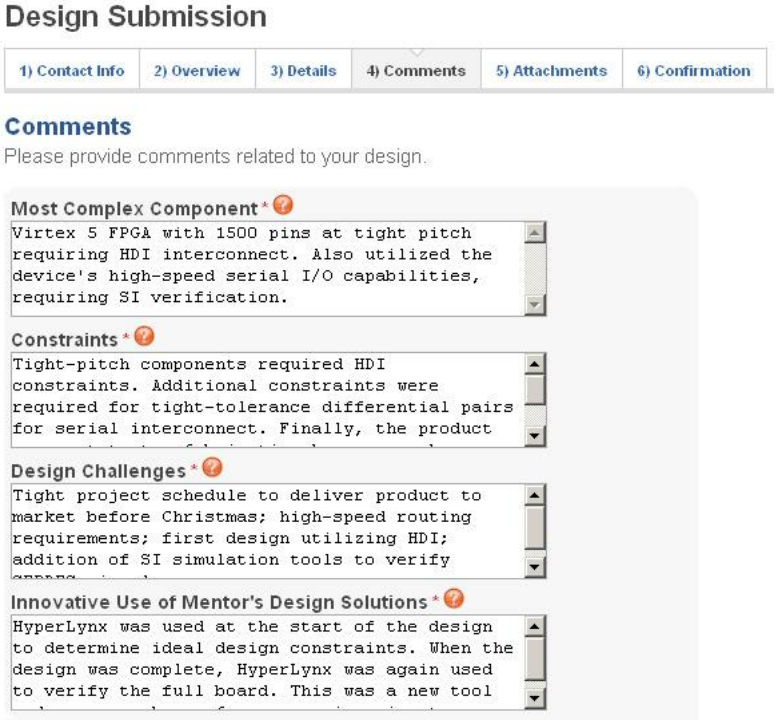
Active Components * 25

Passive Components * 3200

Total Component Area * 45.320 (mm^2)

Number of Component Pins * 16234

Number of FPGAs * 4


Design Submission
1) Contact Info
2) Overview
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4) Comments
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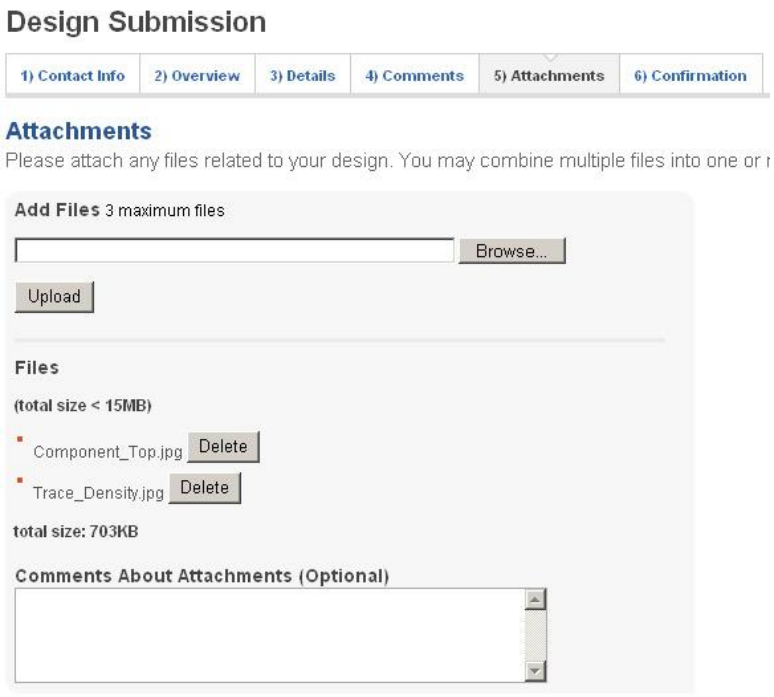
6) Confirmation
Comments
Please provide comments related to your design.
Most Complex Component *
Virtex 5 FPGA with 1500 pins at tight pitch requiring HDI interconnect. Also utilized the device's high-speed serial I/O capabilities, requiring SI verification.
Constraints *
Tight-pitch components required HDI constraints. Additional constraints were required for tight-tolerance differential pairs for serial interconnect. Finally, the product
Design Challenges *
Tight project schedule to deliver product to market before Christmas; high-speed routing requirements; first design utilizing HDI; addition of SI simulation tools to verify
Innovative Use of Mentor's Design Solutions *
HyperLynx was used at the start of the design to determine ideal design constraints. When the design was complete, HyperLynx was again used to verify the full board. This was a new tool


Design Submission
1) Contact Info
2) Overview
3) Details
4) Comments
5) Attachments
6) Confirmation
Attachments
Please attach any files related to your design. You may combine multiple files into one or
Add Files 3 maximum files
Browse...
Upload
Files
(total size < 15MB)
Component_Top.jpg Delete
Trace_Density.jpg Delete
total size: 703KB
Comments About Attachments (Optional)