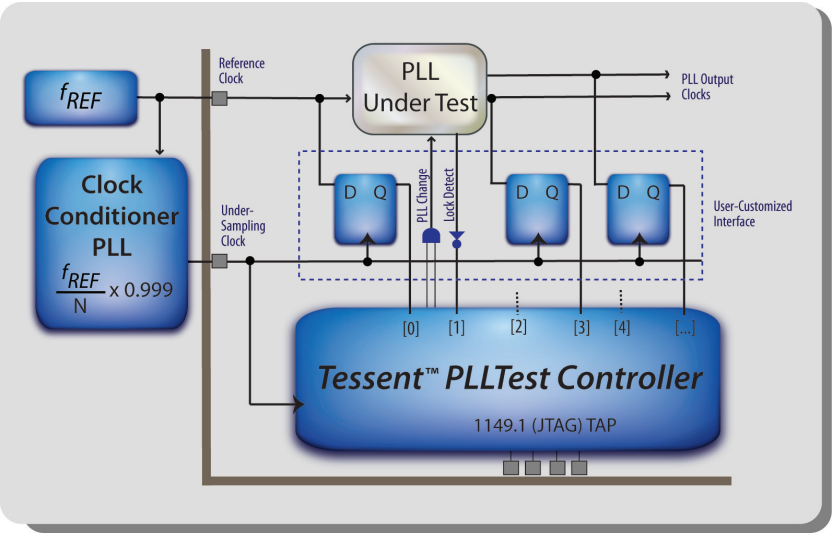
Tessent PLLTest

Parametric Embedded Test for PLLs and DLLs

Silicon Test and Yield Analysis

D A T A S H E E T



Hierarchical Tessent PLLTest infrastructure.

Automated Solution for PLL Test

Mentor Graphics Tessent® PLLTest provides complete, parametric, embedded test for PLLs, DLLs, and clock signals. It can measure jitter, phase delay, duty cycle, frequency ratio, lock time, and lock range, all in less than 100 ms, including test set-up and on-chip comparison to test limits via the IEEE 1149.1 TAP interface. The solution uses Mentor Graphics unlimited time-resolution analysis (ULTRA) patented technology. One 4k-gate ULTRA module can test any number of PLLs, and a TAP controller (or IEEE 1500 WTAP) can interface to any number of ULTRA modules.

Embedded Undersampling-Based Measurement

ULTRA technology uses undersampling to achieve virtually unlimited, silicon-proven time resolution—from 1 second to 100 femtoseconds—using a purely digital analysis logic block synthesized from RTL in a standard digital design flow. Undersampling, when high frequencies are sampled by lower frequencies, is used by most test equipment and is often described as "equivalent time sampling," "mixing down," or "aliasing."

The stimulus data for the PLL-under-test is its normal reference clock (or data), with any amount of jitter. In addition, control of the PLL's internal dividers, using normal functional access, can be exploited to cause the PLL to lose lock or strive for output frequencies at the limit of its lock range.

Key Benefits

- Characterizing with PC plus GPIB-controlled benchtop equipment or microWire-controlled clock conditioner PLL shortens time-to-market.
- Proven picosecond accuracy for any PLL, on any ATE, lowers test cost.
- Diagnostic tests at production speeds improves yield.
- Mentor Graphics award-winning customer support ensures success.

Key Features

- Jitter measurement with pico-second accuracy: Histogram or RMS, timing jitter (loop bandwidth sensitive), period jitter (VCO noise sensitive).
- Phase error and duty cycle measurement with picosecond accuracy: Any number of out-puts, any synchronous output frequency.
- Lock time measurement: Any frequency deviation, single clock-cycle accuracy.
- Design and test automation: RTL insertion and testbench generation, characterization and production tests, repeat-ability analysis.

Mentor Graphics®

Capturing the response is accomplished using simple latches or D-type flip-flops, which may be single-ended or, when measuring sub-picosecond jitter, differential. Sampling is accomplished with a second reference clock having high frequency-resolution and low jitter (differential pins are recommended for measuring jitter less than 5 ps rms, but single-ended routing is usually sufficient). Programming is automated for National Semiconductor's LMK03000 family of clock conditioner PLLs, which may be placed on the ATE loadboard to permit much lower jitter and higher clock frequencies than many ATE can deliver.

All tests can be applied to delay-lock loops (DLLs) and clock signals or any other periodic signals.

Measurement resolution and test time are inversely proportional to the sampling clock's frequency offset from being synchronous to the PLL's reference clock frequency, hence are adjustable and require no calibration.

Lock time is captured by measuring the total duration that the PLL's lock detector indicates loss of lock after the Tessent PLLTest controller initiates a loss of lock by changing the PLL's feedback divider value—lock times up to about 1 second can be measured (test time is limited to the expected lock time). Lock range is verified by loading appropriate input and feedback divider values for the PLL, using normal functional inputs, and then measuring jitter or lock time.

Interactive Debug

Tessent PLLTest includes the Mentor Graphics Tessent SiliconInsight Mixed-Signal solution. With this interactive capability, any of the supported PLL, DLL, and clock signal embedded tests can be run instantly on a PC or tester. The GUI displays all measurement results in engineering units and automatically compares these results to the limits that were shifted into the chip. This allows for detailed characterization and easy setting of production test limits.

Supported Embedded Measurements

- Jitter
  - HF jitter, with LF cut-off frequency controlled by sampling frequency offset.
  - Wideband jitter.
- Phase delay for each output, relative to PLL's reference clock.
- Duty cycle.
- Output to input frequency ratio, for integer or fractional ratios.
- Lock time, based on PLL's lock detector output level after Tessent PLLTest controller-instigated loss of phase lock.
- Lock range, based on acceptable jitter or lock time at selected minimum or maximum PLL output frequencies as generated by loading appropriate values into PLL's dividers.

Tessent Silicon Test and Yield Analysis Solutions

Tessent PLLTest is part of the Mentor Graphics industry- and technology-leading tool suite for silicon test and yield analysis. The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on UNIX and Linux. For more information, visit www.mentor.com.

Visit our website at www.mentor.com

Copyright © 2011 Mentor Graphics Corporation. Mentor products and processes are registered trademarks of Mentor Graphics Corporation.
All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070-7777
Phone: 503-685-7000
Fax: 503-685-1204

Sales and Product Information
Phone: 800-547-3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303

Europe
Mentor Graphics Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1001, 10F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Garden
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140 -0001
Japan
Phone: 81-3-5488-3033
Fax: 81-3-5488-3004

03-11-MGC 1027460