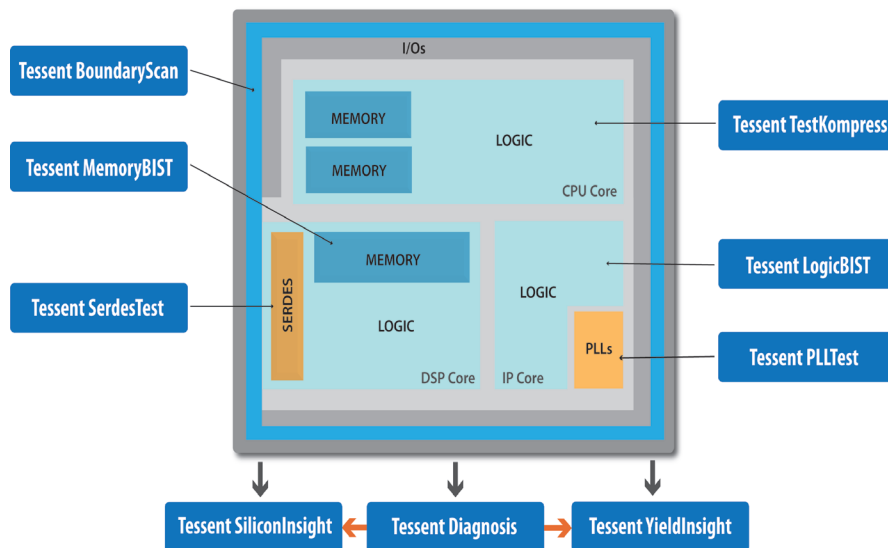


# Tessent

## Comprehensive Solution for Silicon Test and Yield Analysis

### Silicon Test and Yield Analysis

D A T A S H E E T



The Tessent solution tests all aspects of the design to ensure high product quality and cost control.

## Complete Silicon Test Solution

The Mentor Graphics Tessent® product suite provides a comprehensive silicon test and yield analysis platform that addresses the challenges of manufacturing test, debug, and yield ramp for today's SoCs. Built on the foundation of the best-in-class solutions for each test discipline, Tessent brings them together in a powerful test flow that ensures total chip coverage.

## Flexible Test Solutions

The flexibility of the Tessent product line enables the highest quality tests to be applied throughout the product life cycle—from wafer and package test to burn-in, in-system, and field test. Accurate yield analysis is achieved by exploiting the structural nature of scan test and BIST methodologies and correlating to physical features.

## Logic Test

Advanced design techniques used while creating the logic portions of SoCs present significant challenges to achieving high-quality silicon test. To meet these challenges, Mentor Graphics offers the industry's most powerful solutions for logic test: Tessent TestKompress®, Tessent LogicBIST, and Tessent FastScan™. These solutions have more than a decade, and thousands of tape-outs, of successful high-quality test using both compression and vectorless approaches. Together, they provide the maximum flexibility for achieving the most effective test time versus quality optimization.

### Key Benefits

- Comprehensive solutions for logic, memory, mixed-signal, and I/O test achieve very low DPM.
- Diagnosis-driven yield analysis solution significantly reduces cycle time to root cause of yield loss.
- Test debug solution increases productivity during critical silicon validation and debug phases.
- Automated hierarchical test flow ensures minimal impact to design schedules.
- Mentor Graphics award-winning customer support ensures success.

### Key Features

- Provides complete testing through product life cycle, from wafer, package test, burn-in, to in-system and field testing.
- Best-in-class solutions for test compression, logic BIST, memory BIST, and boundary scan.
- Supports testing of 3D-IC designs.
- Unique embedded test and characterization solutions for SerDes and PLLs.
- Uses physical layout data for improved test and yield learning.
- Tight integration between test and yield learning solutions.

## Memory Test

Embedded memory content in SoC designs has increased to over half the area in many designs, and the number of instances and variety of architectures has significantly increased. Further complexity is introduced with multiple clock domains and power islands. Tessent MemoryBIST analyzes the design at the RTL or gate level, identifies test requirements and topologies, determines how many BIST controllers are required, and groups controllers and memories together for sequential or concurrent testing. Designers may choose to implement memory test algorithms as hard-coded or program new ones post-silicon.

One of the most effective ways to significantly improve yield is to repair memories using redundant resources and an on-chip electrical fuse. Tessent MemoryBIST provides a complete memory repair strategy that works with the most popular memory and electrical fuse IP.

## Boundary Scan

Tessent BoundaryScan is a complete solution for the creation and integration of boundary scan cells and related control logic for embedded test and diagnosis of chip I/Os. It also facilitates test and diagnosis of board-level interconnect nets between ICs. Tessent BoundaryScan provides a completely automated solution for adding 1149.1 and 1149.6 boundary scan. It also provides a unique 1149.1-based solution for contactless testing of I/Os.

## Mixed-Signal Test

The Tessent mixed-signal solutions provide complete, parametric, embedded test for PLLs, DLLs, and multi-Gb/s SerDes. The solutions measure waveshape, many types of jitter, and other important performance parameters. The solutions are all based on unlimited time-resolution analysis (ULTRA) patented technology which has been proven on many customer designs operating up to over 10 GHz.

## Managing SoC Test

Tessent SoCScan provides a comprehensive SoC automation flow for easily integrating hierarchical test infrastructure into either the RTL or gate level netlist. The infrastructure includes support for compression and all forms of BIST.

These resources are accessed hierarchically using an IEEE 1149.1 TAP at the chip level and IEEE 1500 core test interfaces at the boundary of each core. The flow provides RTL checking for both ATPG and BIST rules, one step test IP generation and integration, and the automatic creation of all test patterns.

## Silicon Debug and Characterization

Tessent SiliconInsight® reduces test and silicon bring-up time for devices containing Tessent BIST capabilities. The software provides interactive experimentation, debug, and characterization for ATE and benchtop environments.

## Diagnosis-Driven Yield Analysis

During ramp-up of a new product, it can take weeks or even months to identify the root cause of low yield. Tessent YieldInsight® provides advanced statistical analysis and data mining facilities that complement the automated diagnosis capabilities in Tessent Diagnosis. Leveraging manufacturing test results and design data, this solution enables IC manufacturers to identify the probable cause of systematic defects before physical failure analysis. This significantly reduces the time it takes to identify the root cause of yield loss and identifies yield limiters that may otherwise go undetected.

## Tessent Silicon Test and Yield Analysis Solutions

All Tessent tools are available on UNIX and Linux. For more information, visit [www.mentor.com](http://www.mentor.com).

## The Tessent Product Line

### Logic Test

Tessent TestKompress  
Tessent LogicBIST  
Tessent SoCScan  
Tessent FastScan  
Tessent BoundaryScan

### Mixed-Signal Test

Tessent SerdesTest  
Tessent PLLTest

### Silicon Learning

Tessent SiliconInsight  
Tessent YieldInsight  
Tessent Diagnosis

### Memory Test

Tessent MemoryBIST

## Visit our website at [www.mentor.com](http://www.mentor.com)

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**Corporate Headquarters**  
Mentor Graphics Corporation  
8005 S.W. Boeckman Road  
Wilsonville, Oregon  
97070-7777  
Phone: 503-685-7000  
Fax: 503-685-1204

**Sales and Product Information**  
Phone: 800-547-3000

**Silicon Valley**  
Mentor Graphics Corporation  
1001 Ridder Park Drive  
San Jose, California 95131 USA  
Phone: 408-436-1500  
Fax: 408-436-1501

**North American Support Center**  
Phone: 800-547-4303

**Europe**  
Mentor Graphics Deutschland GmbH  
Arnulfstrasse 201  
80634 Munich  
Germany  
Phone: +49.89.57096.0  
Fax: +49.89.57096.400

**Pacific Rim**  
Mentor Graphics Taiwan  
Room 1001, 10F,  
International Trade Building  
No. 333, Section 1, Keelung Road  
Taipei, Taiwan, ROC  
Phone: 886-2-87252000  
Fax: 886-2-27576027

**Japan**  
Mentor Graphics Japan Co., Ltd.  
Gotenyama Garden  
7-35, Kita-Shinagawa 4-chome  
Shinagawa-Ku, Tokyo 140-0001  
Japan  
Phone: 81-3-5488-3033  
Fax: 81-3-5488-3004

