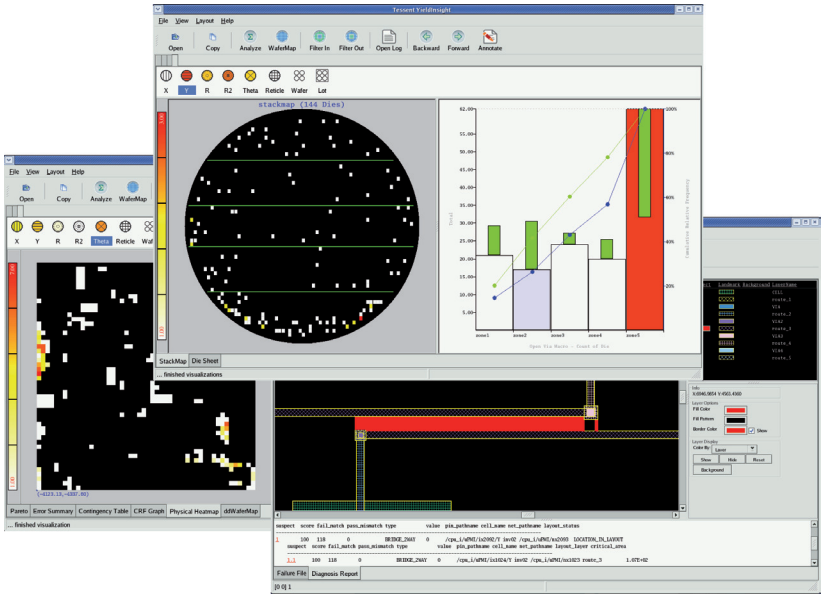
Tessent YieldInsight

Diagnosis-Driven Yield Analysis

Silicon Test and Yield Analysis

D A T A S H E E T



Tessent YieldInsight identifies the cause of systematic yield loss and provides guidance through the process of selecting die for failure analysis.

Leveraging Test for Yield Analysis

At technology nodes of 65 nm and smaller, ramping and maintaining high yield is a challenge. Manufacturing processes are still being characterized, and the interactions between the physical processes and design features can be extremely subtle and difficult to identify. Feature-related systematic defects are slowing yield ramp, putting a crunch on time to market—and maintaining expected yield is more difficult, putting added pressure on profitability.

Not only are more devices failing because of hidden systematic defects, but increased sensitivity to manufacturing variability is resulting in functional and parametric yield loss. In order to keep pace, manufacturing test and yield analysis processes must adapt.

The Mentor Graphics yield analysis solution, Tessent® YieldInsight®, analyzes large populations of scan diagnosis reports to intelligently and quickly identify the most likely yield loss mechanisms. The software uses innovative design-correlated analysis methods that supplement traditional fab-centric yield management systems. In a manner consistent with yield and failure analysis tools, it steps through the process of selecting and filtering populations of failing die, grouping die that are failing for similar reasons, and analyzing various aspects of these populations to identify and locate systematic yield loss mechanisms.

Key Benefits

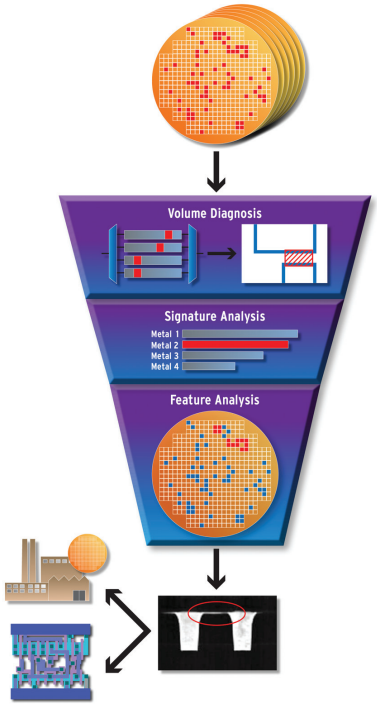
- Significantly reduce cycle time to root cause of yield loss.
- Automatically identify hidden yield limiters.
- Identify observable yield problem with test and diagnosis results visualization.
- Improve device selection for failure analysis, maximize success rate and relevance.
- Identify DFM rules that best describe design-process induced systematic defects
- Prioritize yield enhancement efforts.
- Mentor Graphics award-winning customer support ensures success.

Key Features

- Dashboard indicates presence of systematic defects based on statistical test of independence for eight zonal types.
- Drill-down capability to effectively pick die for failure analysis.
- Pareto plot and analyze more than 70 failure and diagnosis signatures.
- Filter in/out capability to analyze select material.
- Flexible wafer stack maps.
- Pareto charts.
- Cumulative relative frequency (CRF) graphs.
- Failing scan cell intensity maps.
- Die-level defect intensity maps (heat maps).
- Physical suspect viewer.
- TCL command interface provides low-level access to all data.

Advancing Yield Analysis

Tessent Diagnosis is able to effectively diagnose large volumes of production test failures. Tessent YieldInsight statistically analyzes this data to identify and separate systematic yield limiters before any failure analysis is done. This eliminates the need for costly physical localization and reduces the time to determining root cause of yield loss from weeks to days.



The diagnosis-driven yield analysis flow includes production test diagnosis and statistical analysis.

Tessent YieldInsight organizes the data based on diagnosis and failure signatures. Using industry-standard visualization tools such as stacked wafer maps, like devices are separated and the most common failure features identified to determine the cause of observable yield loss.

Tessent YieldInsight automatically performs statistical tests of independence of all the signatures across several zonal types. The software identifies the most variant features, i.e., the failure mechanisms that have an unexpected distribution and therefore require investigation.

For example, the total distribution of defects across the wafer may appear random, while open defects containing via3 occur primarily in the center of the wafer. Even though via3 opens is not the most common defect type, this type is of interest because of the unexpected distribution. Tessent YieldInsight uses zonal analysis to automatically identify this type of hidden yield limiter.

Selection of die for failure analysis is facilitated by automatically identifying die that clearly exhibit the identified systematic issues. This accelerates yield ramp compared to traditional techniques.

Resolving design-process induced systematic defects is one of the few ways that fabless semiconductor companies can directly improve yield. Layout-aware diagnosis results can be correlated with Critical Feature Analysis (CFA) results to Design for Manufacturing (DFM) violations that best describe the actual yield limiters.

Tessent Silicon Test and Yield Analysis Solutions

Tessent YieldInsight is part of the Mentor Graphics comprehensive silicon learning solution:

- Tessent SiliconInsight® reduces test and silicon bring-up time with interactive debug and characterization.
- Tessent YieldInsight accelerates yield ramp and time to root cause of yield loss with visualization and statistical analysis of scan test data and diagnosis results.
- Tessent Diagnosis provides defect and timing error identification for debug, failure analysis, and high-volume yield analysis.

The Tessent suite includes integrated solutions for test insertion; automatic test pattern generation (ATPG); on-chip compression; memory, logic, and mixed-signal built-in self-test (BIST); silicon bring-up, and diagnosis-driven yield analysis. All Tessent tools are available on UNIX and Linux. For more information, visit www.mentor.com.

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