

# Advanced Scan Diagnosis Based Fault Isolation and Defect Identification for Yield Learning

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## **Abstract**

*Yield analysis of sub-micron devices has become an ever-increasing challenge. The difficulty is compounded by the lack of in-line inspection data as many companies adopt foundry or fab-less model. In this scenario failure analysis is becoming increasingly critical to help drive yields. Failure analysis is a process of fault isolation or a method of isolating failures as precisely as possible followed by identification of a physical defect.*

*As the number of transistors and metal layers increase, the traditional fault isolation techniques are becoming less applicable and un-economical due to the amount of time needed to locate the physical defect. One solution to the yield analysis problem is scan diagnosis based fault isolation. Previous scan diagnosis based techniques were limited with little information about the type of fault and accuracy of diagnosis. With the introduction of new scan diagnosis algorithms it is now possible to not only isolate but to identify the type of fault as well as assigning an accuracy ranking, prior to any destructive analysis.*

*This paper presents multiple case studies illustrating the application of scan diagnosis as an effective means to achieve yield enhancement. The advanced scan diagnostic tool utilized in this study provides information about the fault type as well as fault location. This information is used to focus failure analysis efforts toward a suspected defect, decreasing the cycle time required to determine root cause as well as increasing the over all success rate.*

## **1 Introduction**

Yield analysis has traditionally been a process of identifying wafers with lower than expected yields and then attempting to isolate the causes of failure through correlations to in-line inspection, scribe-line structures, and memory bitmapping or failure analysis.

As many companies move to foundry/fab-less models, more emphasis is being placed on failure analysis to help drive yields.

Traditional fault isolation techniques such as emission microscopy, OBIRCH, liquid crystal are becoming more difficult as technologies become denser and the number of metal layers increases.

Emission microscopy from the front side is proving increasingly challenging as the number of metal layers increase. Backside emission analysis is not always possible, due to either packaging or socketing issues. As devices scale, the background IDD increases making it even more difficult to isolate subtle defects with emission analysis. OBIRCH only works if the suspected node can be excited, which is difficult as the number of layers increases. Liquid crystal analysis does not have the resolution to identify a single cell if you even get an area of elevated temperature through the background heat dissipation. A large amount of time can be spent tracking a suspected defect if the defect is not isolated accurately.

Memory bit mapping isolates the defect very precisely and with little interpretation the defect type can be determined with a high degree of accuracy. The only draw back to memory analysis is the fact that most memories are routed in the lower layers of a device, biasing the types of defects that can be observed.

One solution to the challenge of yield analysis is the use of scan diagnosis based fault isolation techniques. Scan diagnosis based fault isolation is not a new concept, on the contrary it have been proven a successful tool in the failure analysis world.

The problem with traditional scan based approaches is that the isolation was not much better than that of photoemission isolation techniques. Once a scan failure was identified and analyzed, a list of suspected nodes was generated. The analyst would then spend a large amount of time trying to further isolate the possible fault location and defect type by comparing the list of suspected nodes against the circuit schematic and physical layout. The analyst would then have to make an educated guess as to the type of defect that may be present and how to continue with physical failure analysis based on these assumptions. In addition, traditional scan fault model based algorithms in scan diagnosis were biased toward “stuck at” type defects, making it much more difficult to identify open and bridging type defects.

With advances in scan diagnostic algorithms and more in depth fault modeling many of the difficulties associated with scan diagnosis analysis have been eliminated leading to higher success rates and a significant decrease in cycle time.

This paper is organized as follows. Section 2 provides information about the advanced scan diagnosis tool used for this paper. Experimental setup is described in Section 3, whereas results are outlined in Section 4. Finally conclusions are provided in Section 5.

## 2 Advanced Scan Diagnosis

Scan based diagnosis is a mature concept that is routinely used for fault isolation on individual failures [1-6]. Recently it has also been shown applicable to yield improvement [7-9]. The diagnosis tool employed for this study is suited for analysis of one-of-a-kind failures as well as failures from manufacturing that can be used for yield learning.

Yield learning requires a high performance diagnosis tool to process statistically sufficient failure data. Besides performance, the key features of a scan diagnostic tool necessary to drive yield learning efforts are defect classification and suspect ranking.

The diagnosis tool utilized for this study uses a location-based approach to identify the suspects. In addition it also classifies the suspects and assigns a score for each suspect indicating how well the suspect behavior matches with the observed failures on the tester. The general flow of this approach is: first, for each failing pattern, it simulates each single gate pin location with failure (the location has opposite logic value from good machine value) to see whether the failing pattern can propagate the failure to all observable points with same behavior as observed on the ATE. If the scan diagnosis tool finds any correlation, the failing pattern is explained by

that location. After this step, a heuristic method is used to find a set of minimal faults that can explain all the failing patterns. The heuristic method can be minimum set covering algorithm [14, 15], or probability based method [16].

Furthermore, the diagnostic tool separates all fail data into several independent *symptoms*. For each symptom, it lists the suspects that explain the failing patterns in that symptom. New diagnostic algorithms are added to classify all suspect behavior and a formula is used to give a score for each suspect such that for each symptom, all suspects are ranked.

### 2.1 Suspect Type

The tool that was used for this experiment classified all suspects into the following categories:

Stuck-At – A stuck-at 0 or stuck-at 1 suspect which explains not only the failing patterns but also all passing patterns.

Open/Dom Bridge – This category is used for suspects that fail both a 0 and 1 state during different patterns. The defect could be due to an open or a dominant bridge to another signal.

B-OR – A 2-way bridge that acts as a wired-OR logic failure. A 1 on either signal causes both signals to pull to a 1.

B-AND – A 2-way bridge that acts as a wired-AND logic failure. A 0 on either signal causes both signals to pull to a 0.

3-Way Bridge – A bridge affecting 3 lines.

EQ# – The suspect is equivalent to another suspect listed above whose number is #.

Indeterminate – The suspect was not discernable with the available information.

### 2.2 Suspect Ranking

Besides identifying suspect types, the new algorithm gives a score to each suspect based on a formula that calculates the similarity of simulated behavior versus what was observed on the ATE. It should be noted that different suspect types have different simulated behavior even if they are at the same logical location. For example, a bridge suspect should have less failing patterns than a stuck at suspect at the same location. The score is normalized from 1 to 100 with the higher the better. Based on the scores, all suspects of each symptom are ranked. The tool has an option to list the percentage of suspects of each symptom. By default, it only lists the suspects with score higher than 80 or ranked top three of each symptom.

### 2.3 Diagnosis output

Figure 1 shows a sample scan diagnosis output. It begins with tracking information section for failing die, which if included in the failure file would appear as is in the diagnosis report between the keywords tracking\_info\_begin and tracking\_info\_end. Next is the global information section about diagnosis such as total number of symptoms, total number of suspects, CPU time spent on diagnosis, input failure file information, and finally number of failing patterns, number of passing patterns, and number unexplained failing patterns. If there are any unexplained failing patterns, their numbers are listed as well. Information about each symptom is then listed. For each symptom, its ID, number of suspects for that symptom and the number of failing patterns explained by that symptom as well as failing pattern numbers is provided. Following this is the list of suspects for that symptom. For each suspect, its ID, score, type, value and location composed of pin path name, cell name, net path name are provided. All suspects within a symptom explain the failing patterns listed for that symptom. Their score reflects how well they explain the passing patterns in addition to the failing patterns. A suspect with a score of 100 perfectly explains all the failing patterns and passing patterns. In cases where a failing device has multiple defects the diagnosis report contains multiple symptoms.

```
tracking_info_begin
tracking_info_end
#symptoms=1          #suspects=1          CPU_time=5.76sec
fail_log=fail_logs/X59Y61.log.nochain.mentor

#failing_patterns=5, #passing_patterns=263
#unexplained_failing_patterns=0

symptom=1 #suspects=1 #explained_patterns=5
12 28 35 110 239
suspect score type    value pin_pathname (cell_name) (net_pathname)
-----
1      100 STUCK    0   /m_1/m_55/B (NR2M2D) (/m_1/pi26)
```

Figure 1: Scan diagnosis output example

### 3 Experimental Set up

A test chip was selected for use during ongoing yield analysis. This test chip was built on a CMOS .11µm low-K technology with 6 layers of metal routing. Failures were logged for scan diagnostics. The number of failures to data log is crucial. If too few failures are collected the

diagnosis may not be as accurate but if too many failures are collected the amount of test time and therefore test cost can increase drastically. For the purposes of this experiment 200 failing cycles were collected for each failing device.

## 4 Results

Scan diagnostics were performed on 12 failing devices. The advanced scan diagnosis algorithm was able to identify possible fault locations on 10 of the 12 devices.

Seven devices were diagnosed with suspects having a rank of 100, the remaining 3 devices all contained suspects of rankings between 70 and 90. In the following subsections results for two cases are explained in more detail.

### 4.1 Case 1

For case 1, diagnosis identified two possible suspect candidates as illustrated in Figure 2. Suspect 1 is identified as a STUCK 0 on the Z output of a NAND gate. Suspect 2 is identified as a STUCK 0 on the A input of an XNOR gate. The advanced scan diagnosis algorithm lists the second suspect type as EQ1, indicating the second suspect location is equivalent to suspect location one.

```
tracking_info_begin
tracking_info_end
#symptoms=1          #suspects=2          CPU_time=6.50sec
fail_log=fail_logs/X61Y63.log.nochain.mentor
#failing_patterns=141, #passing_patterns=122
#unexplained_failing_patterns=0

symptom=1 #suspects=2 #explained_patterns=141
1  8  9 10 11 12 13 17 18 19
20 22 23 24 26 27 30 34 36 37
38 39 40 41 42 43 44 45 46 48
49 50 51 52 53 55 58 64 65 67
68 71 73 74 75 77 79 81 83 85
86 87 88 89 90 95 96 98 99 100
102 108 112 114 116 139 140 142 144 145
148 149 151 153 154 156 157 158 160 162
163 166 167 168 169 170 171 172 174 175
176 177 178 179 180 181 184 185 187 188
189 190 191 193 194 196 198 199 200 203
205 206 209 210 212 213 214 215 216 218
219 220 221 222 227 228 231 239 241 242
243 244 247 248 249 250 253 254 259 260
262
suspect score type    value pin_pathname (cell_name) (net_pathname)
-----
1      100 STUCK    0   /a0/m_4/U130/Z (ND2M1D) (/a0/m_4/w_285)
2      100 EQ1      0   /a0/m_4/U129/A (ENM1D) (/a0/m_4/w_285)
```

Figure 2: Case 1 scan diagnosis output

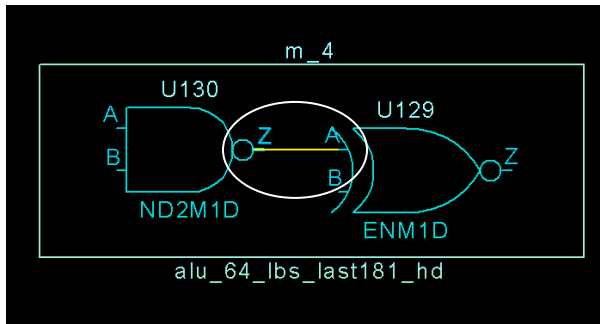


Figure 3: Case 1 fault candidate schematic.

Figure 3 shows the schematic of the identified fault candidates. Notice the Z output of the NAND gate drives the A input of the XNOR gate with no additional fanouts. This is the reason the algorithm identifies both locations, meaning the physical defect may be internal to either the XNOR, NAND or metal routing between. With the fault isolated the remaining analysis can now be focused on the two suspect logic gates prior to any destructive analysis. Physical layout analysis of the identified net between the two logic gates revealed the net of interest is routed at the metal 3 layer and below.

A chemical deprocessing technique was used to remove the upper layers of thick metal. A parallel lapping technique was then used to remove the remaining layers of oxide and metal to expose the metal 3 net of interest.

The faulty node was electrically evaluated using SEM in chamber nano probes. Figure 4 shows the IV curve of an NP junction diode observed on the suspected node. At the layer the device was electrically evaluated the Z output of the NAND gate was intact and should exhibit both an NP and a PN diode known as the “Double Diode Curve”.

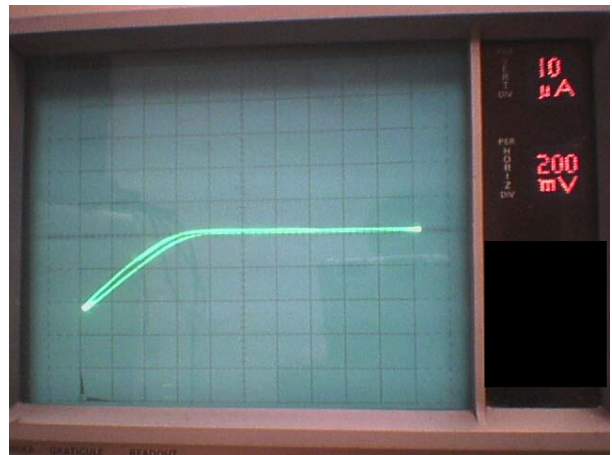


Figure 4: Case 1 I/V curve of node identified by scan diagnosis.

Additional physical layout analysis of the driving NAND revealed single contacts to both N and P active outputs. It was determined that an open P active contact would cause both a stuck-at 0 signature and yield only an NP diode. FIB cross section analysis of the suspected P active contact confirmed the P active contact to be unlanded due to a blocked etch as illustrated in Figure 5. It is important to note that the defect is an open but due to its location in the circuit it acts as a stuck at defect. After the scan failures were collected and diagnosed the root cause analysis on this failure was completed within four hours.

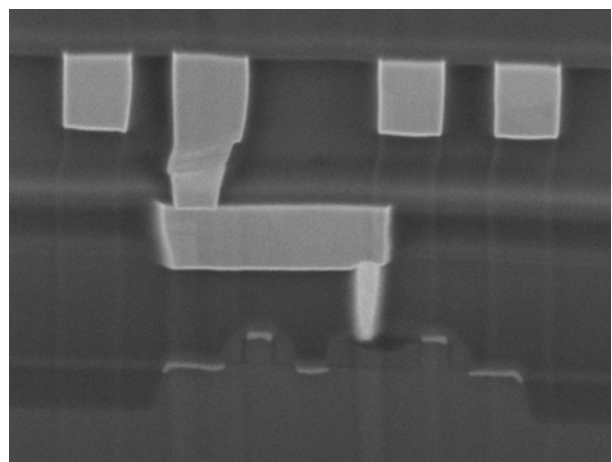


Figure 5: Case 1 cross section of open P active contact leading to a stuck-at 0 scan failure.

## 4.2 Case 2

Diagnosis identified three separate nodes as possible fault locations for case 2. From the diagnosis output illustrated in Figure 6 it can be seen that all three possible suspect locations received different rankings. All suspects belong to the same symptom, meaning there is only 1 defect causing the failure but it can only be isolated to within 3 nodes. Figure 7 shows the schematic of the three suspect nodes. A quick glance at the schematic confirms that the diagnosis algorithm could not further isolate a defect on one of the three suspected nodes.

```

tracking_info_begin
tracking_info_end
#symptoms=1                #suspects=3                CPU_time=7.81sec
fail_log=fail_logs/X61Y62.log.nochain.mentor
#failing_patterns=114, #passing_patterns=154
#unexplained_failing_patterns=0

symptom=1 #suspects=3 #explained_patterns=114
6  9  10 11 12 13 14 15 17 19
21 24 27 29 30 33 34 35 37 38
44 45 47 48 49 51 53 58 59 61
63 66 67 68 70 71 72 74 76 77
78 79 80 82 86 88 89 90 92 97
98 101 102 104 105 108 112 113 116 139
140 157 158 160 163 169 170 175 176 180
181 182 183 186 187 188 189 194 199 200
206 212 213 215 216 219 221 223 224 225
229 231 232 234 236 238 241 242 243 245
247 248 249 250 251 252 254 255 260 261
263 264 265 267
suspect score type      value pin_pathname (cell_name) (net_pathname)
-----
1      86  OPEN/DOM  both /a0/m_4/U46/Z (ND2BNM1D) (/a0/m_4/w_491)
2      81  OPEN/DOM  both /a0/m_4/U200/Z (ENM1D) (/a0/m_4/f57)
3      73  OPEN/DOM  both /a0/m_4/U201/Z (ND2M1D) (/a0/m_4/w_489)

```

Figure 6: Scan diagnostic output for Case 2

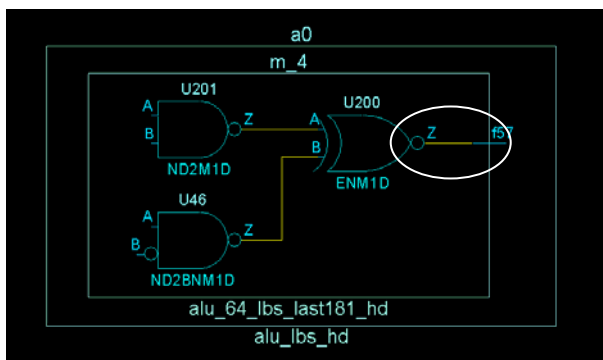


Figure 7: Case 2 fault candidate schematic

A chemical deprocessing technique was used to remove the upper layers of thick metal. A parallel lapping technique was then used to remove remaining layers of oxide and metal to expose the metal 4 layer

of interest. SEM in chamber nano probes were used to confirm the proper IV curves on suspect 1 and 3 no IV curves could be obtained for suspect 2, indicating an open between the metal 4 probe location and the driving XNOR logic gate. FIB isolation cuts in conjunction with SEM PVC and nano probe electrical verification narrowed the source of the open to a single VIA 2. FIB cross-section analysis of the suspected VIA 2 confirmed the presence of a void located in the middle of the VIA 2. After scan failures were collected and diagnosed the root cause analysis on this failure was completed within four hours.

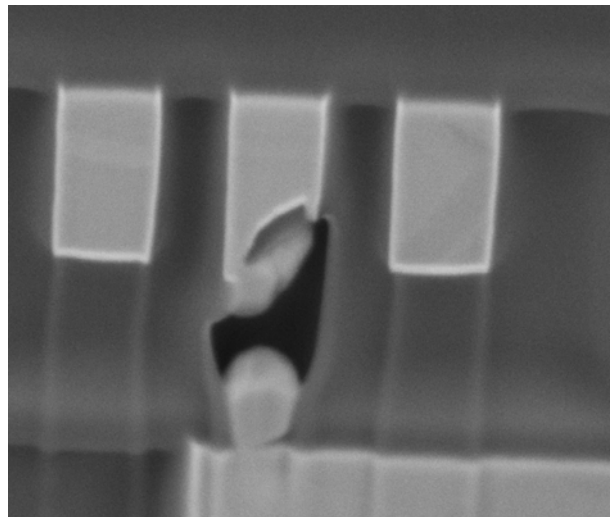


Figure 8: Case 2 Cross section of Open VIA 2 located on defect number 2 causing an open failure.

**Note: Additional case studies will be added in final draft.**

## 5 Conclusion

Yield analysis is a crucial part of the fabrication process. Providing accurate and timely data to a fab has proven to be invaluable when attempting to increase device yields. With the aid of advanced scan diagnosis based fault isolation with suspect type identification and scoring, the flow of an analysis can be modified to increase the root cause success rate while decreasing the amount of time spent per analysis.

## 6 References

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