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Test Compression

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Scan technology is essential for testing the digital content of large-volume devices. By using scan, you can make the device itself responsible for some of the “test” chores, and you can shorten the time needed for automatic test pattern generation. The key to setting up a successful scan-test operation is deciding exactly how much scan compression an application needs.

In scan-test mode, scan structures allow each sequential gate to be concatenated with other sequential gates and configured as a long shift register called a scan chain. Each sequential gate can be loaded with a predefined value and treated as a control point.

Once the device captures values into the sequential elements, an automated tester can enable scan test and “observe” results.

Instead of trying to create patterns for a complex sequential circuit, all sequential gates behave as control and observe points. Overall, the test problem is reduced to testing the small blocks of combinational logic between the sequential gates. Scan simplifies the test problem enough that automated test pattern generation (ATPG) tools can quickly and efficiently create test patterns.

Increases in test volume

Historically, as devices grew in gate count, scan test data volume and application time grew as well. A device that contains twice as many gates as the previous generation has scan chains that are twice as long, unless more scan chains are added. This is due not only to larger designs but also to the additional pattern types necessary to detect newer defect mechanisms. At the same time, these larger designs are moving to more modular and hierarchical design methodologies, creating the demand for fewer test signals from each circuit block.



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As a result of the emergence of new fabrication technologies, standard stuck-at scan tests are no longer sufficient. Many companies have seen significant growth in the number of timing-related defects at 130 nm and below. At-speed scan testing has become necessary to detect this growing population of defects, but unfortunately, the most popular approach for at-speed scan requires a more complex pattern.

The most desirable application of at-speed scan test involves loading values into the scan chains at a slow clock rate and then applying two cycles at the system clock frequency. At-speed patterns can use internal PLLs for the at-speed launch and to capture pulses to provide accurate clocking. Because two cycles are required in the functional mode of these tests, at-speed scan patterns are typically three to five times larger than a stuck-at pattern set. Note that ATPG tools can support at-speed scan tests that are simpler and require fewer patterns—these are called launch-off-shift patterns. Such tools impose more design constraints, however, and will test more nonfunctional logic, possibly reducing yield.

In addition to using at-speed scan testing, some companies are starting to apply tests that target specific types of defects or the physical locations where certain defects are most likely to occur. One new pattern type statistically targets bridge defects that may have escaped stuck-at pattern tests. The idea is to detect a fault at each gate terminal multiple times while randomly changing how the fault is detected. This pattern type is referred to as multiple-detect pattern and can be created for stuck-at and transition faults.

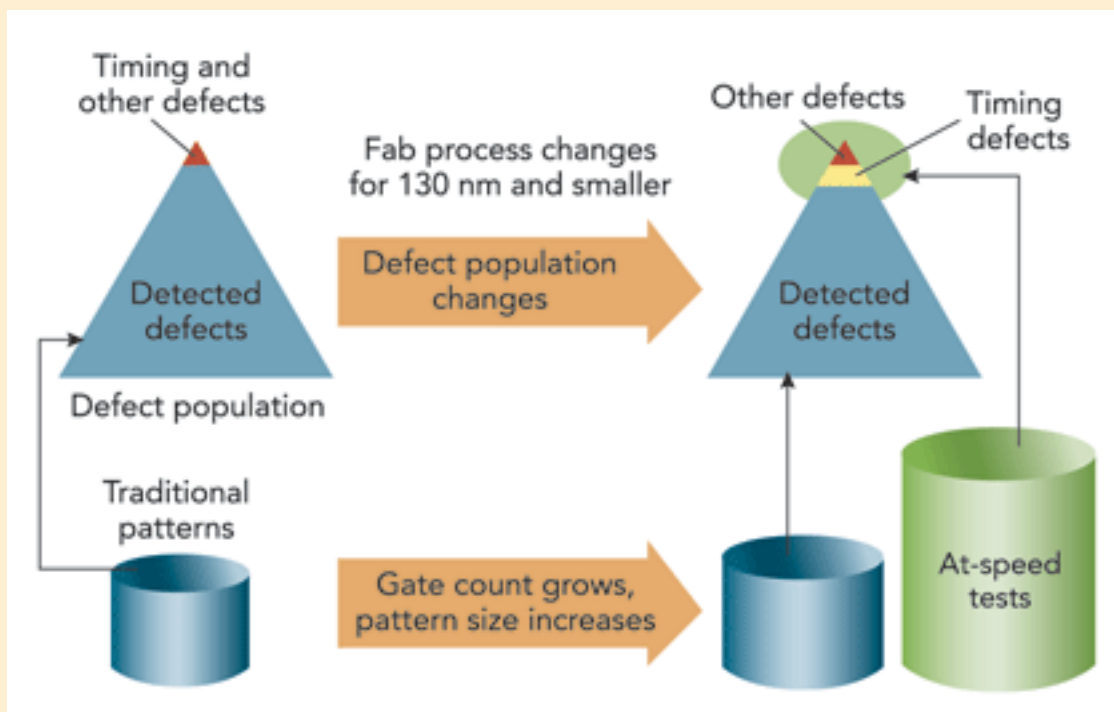


Figure 1. New tests related to timing are needed to cover new defects introduced by fab process changes.

Another new family of tests is based on targeting physical locations within the device layout database (GDSII) to identify the most likely defect locations. Since these tests use design-for-manufacturing

(DFM) layout rules to identify the likely defect locations, they are often called DFM-based fault model tests. The first such fault model to be used is based on bridge extractions, and some manufacturers are using a combination of multiple-detect patterns and deterministic bridge extraction patterns (Figure 1).

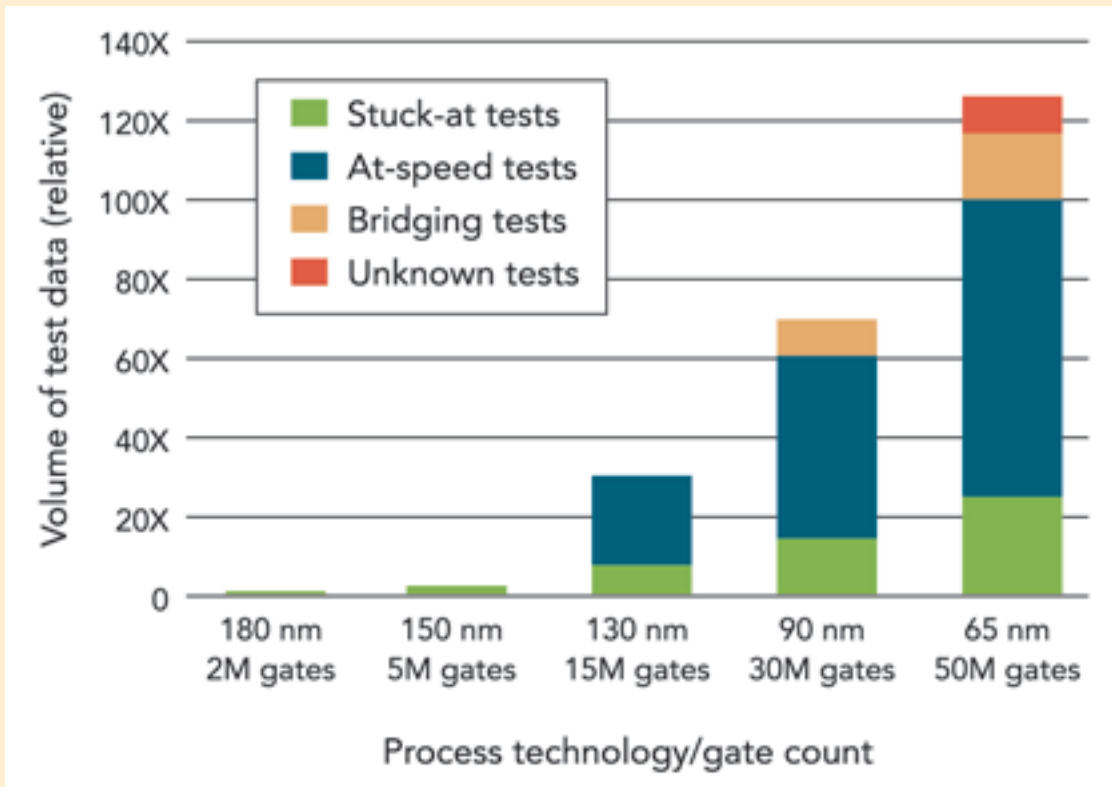


Figure 2. The number of tests and corresponding data volume increase with each new fabrication process technology.

As fabrication technologies evolve, test application time and test data volume are drastically increasing just to maintain test quality requirements (Figure 2). For example, new tests require:

- greater than 2X the test time to handle devices that double in gate count but maintain the same number of scan channels,
- 3X to 5X the number of patterns to support at-speed scan testing for the growing population of timing defects at 130-nm and smaller fabrication processes, and
- 5X the number of patterns to handle multiple-detect and new DFM-based fault models.

This equates to a minimum of 10X compression for increased design sizes and at-speed test patterns just to maintain quality and tester throughput. If newer multiple-detect or DFM-based fault models are added, then the test time will increase to 20X.

Thus, the starting point is 10X compression just to maintain tester throughput and 20X if new fault models are used, which becomes 40X if the next design doubles in size. If you consider reducing the block-level routing and top-level scan pins by 5X, that means you need 5X more compression on top of the existing compression. Supporting multisite testing or DFM-based fault models will triple the

compression requirements at a minimum. A major benefit of compression is to reduce test pin count, which is a major cost benefit at manufacturing. As a result, some companies are already looking for compression well beyond 100X tester cycle reduction.

Test-compression techniques

A few important factors to consider with any compression technique are:

- the amount of compression possible,
- the scalability of compression (does the compression technique work with various design sizes, with few or many scan channels, and with different types of designs?),
- the robustness in the presence of X states (can the design maintain compression while handling X states without losing coverage?), and
- the ability to perform diagnostics of failures when applying compressed patterns.

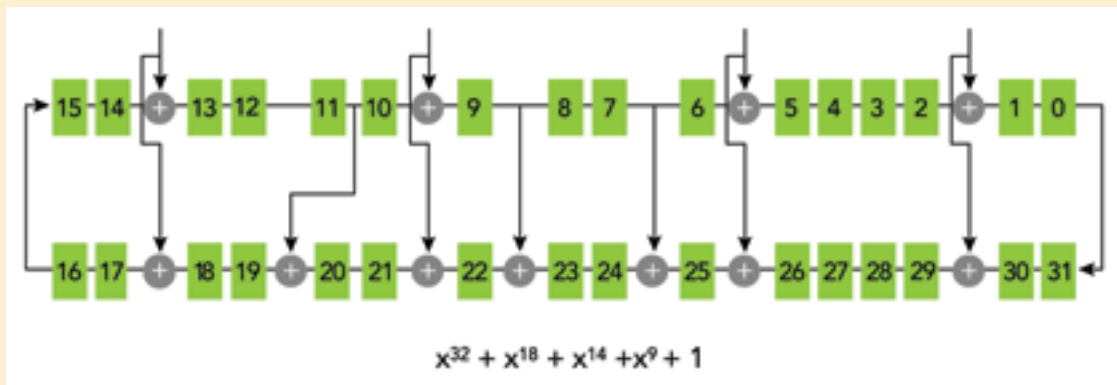


Figure 3. The embedded-deterministic-test decompressor shown here employs a continuous-flow ring generator.

Popular scan techniques include Illinois Scan, a technique that involves connecting many internal scan chains to a common scan channel, and embedded deterministic test (EDT), which employs a combination of approaches to provide high compression while working in the presence of X states. The input side is called a continuous-flow ring generator (**Figure 3**). It is similar to a linear feedback shift register (LFSR) in that it can produce random data, but the device is used to decode compressed data with every shift of scan channel values.

In Mentor Graphics' EDT implementation (see Web-exclusive sidebar "[Modular embedded deterministic test](#)"), the initial ATPG process of determining which values to load into scan cells to detect as many faults as possible is exactly the same as in standard ATPG. This is true for any type of scan pattern. But if standard ATPG were used, it would use random values to fill up the unspecified scan cells that cannot improve targeted fault detection.

Instead, EDT processes the desired specified bits for the pattern and determines how to load them through the decompressor. When the resulting compressed pattern is loaded through the decompressor, the specified bits get loaded into their respective scan cells. A side effect of the

decompressor is that all the unspecified bits get loaded with random data. As a result, lots of tester cycles are saved by not having to specifically load random data.

In a tester using EDT, scan-chain outputs feed into a compactor. Several scan chains are XOR-combined into individual scan channels. Each scan chain only propagates to one gate with this configuration, which controls routing congestion.

One of our most important considerations when developing the EDT architecture was how to handle X states. Even if no X's are present in the design, the design may still need to accommodate X's when considering false and multicycle paths for at-speed patterns. Other-wise, there could be huge losses in test coverage and compression.

The EDT compactor has a masking capability at each scan chain output (**Figure 4**). Masking is only used when a fault that was specifically targeted is disrupted by an X propagating to the same scan channel. EDT determines when masking is needed automatically during pattern generation. Values are loaded into the mask register during scan chain loading so no special tester protocol is needed. The decompressor treats the values as specified bits that are automatically solved during pattern generation.

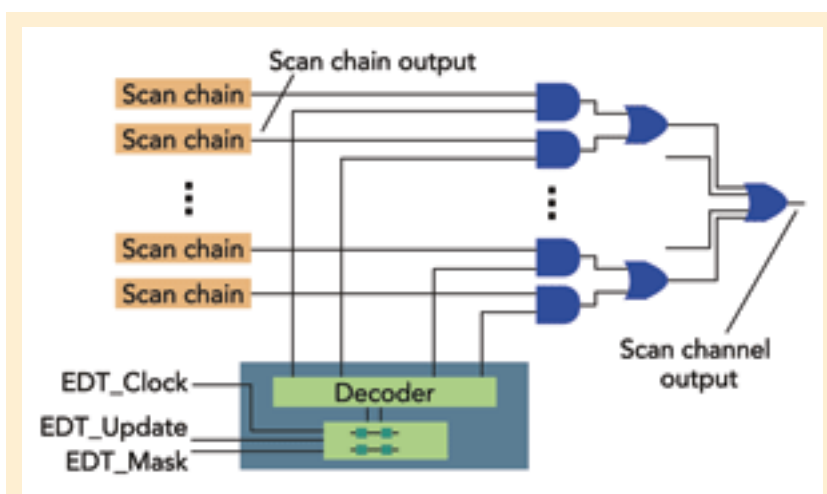


Figure 4. An EDT compactor can mask unknown states from disrupting fault detection.

In EDT, many internal scan chains are loaded through a small interface of several scan channels. The ratio of internal scan chain to channels defines the maximum possible compression. EDT provides the following capabilities:

- very high levels of compression—many devices have been designed with effective compression in the 100X range;
- scalability—effective compression is possible with just one scan channel and has been used in smart cards that have only a three-pin test interface;
- compressed pattern diagnostics;
- no loss of coverage in the presence of X states, making possible the masking capability; and
- flexibility—the EDT logic is only based on the number of scan chains and works as a transform function (with no need to change the EDT logic due to core design changes as long as the number and interface to scan chains remains constant).

Table 1. Illinois vs. EDT scan effectiveness

| DESIGN | GATES | METHOD | COVERAGE | VOLUME | COMPRESSION |
|--------|-------|----------|----------|--------|-------------|
| A | 543k | ATPG | 98.83% | 61M | 1.0 |
| | | Illinois | 97.45% | 2.8M | 21.9 |
| | | EDT | 98.85% | 1.3M | 46.8 |
| B | 576k | ATPG | 98.71% | 75M | 1.0 |
| | | Illinois | 98.48% | 2.1M | 35.5 |
| | | EDT | 98.71% | 1.3M | 57.0 |
| C | 1.2M | ATPG | 97.06% | 578M | 1.0 |
| | | Illinois | 96.75% | 10M | 57.3 |
| | | EDT | 96.99% | 7.7M | 75.6 |
| D | 1.2M | ATPG | 99.88% | 25M | 1.0 |
| | | Illinois | 95.16% | 2.7M | 9.2 |
| | | EDT | 99.86% | 0.8M | 32.1 |
| E | 1.5M | ATPG | 99.04% | 59M | 1.0 |
| | | Illinois | 98.17% | 2.8M | 21.5 |
| | | EDT | 99.03% | 1.6M | 38.1 |
| F | 2.1M | ATPG | 98.86% | 193M | 1.0 |
| | | Illinois | 96.95% | 11.7M | 16.5 |
| | | EDT | 98.84% | 4.3M | 44.8 |

To demonstrate the compression value of EDT technology, we evaluated six designs using both ATPG without compression, EDT, and Illinois Scan (**Table 1**) with the same scan-chain-to-channel ratio on the input side. For accurate comparison, no compaction was used on the output.

We found that the highest coverage using standard ATPG was reached by EDT for all six designs. Also, the EDT compression ratio (normalized for the coverage achievable by Illinois Scan) is noticeably better. As a result, a design configured with EDT compression logic can accommodate more patterns of various types within the same tester data volume and test application time. Even greater compression can be achieved by using the EDT compactor on the output that is capable of masking unknown states. Using a compaction technology without masking can result in huge coverage loss and lower compression.

Modular embedded deterministic test

An additional feature added to Mentor Graphics TestKompress EDT tool to support block-based design is called Modular EDT. It allows EDT to be completely inserted within design blocks such that no logic is necessary at the design top level. As a result, each block can have as few as one scan channel and share the EDT control signals—EDT clock, scan enable, and an edt_update signal.

Large designs with high levels of compression will often use Modular EDT. Consider the following example. 50,000 scan shifts were necessary to load 20 scan chains for each pattern. This could potentially reach 100X compression if EDT is implemented with 3000 scan chains, but this would require routing of 3000 scan chains to the EDT decompressor and compactor. Instead, modular EDT can be used in 10 design blocks with each block having only 300 routes to the EDT logic within it. Modular EDT can test all blocks in parallel at the design top level. This is true for blocks without EDT and only traditional scan as well as blocks with a mixture of traditional and EDT scan.—*Ron Press and Jay Jahangiri, Mentor Graphics*

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